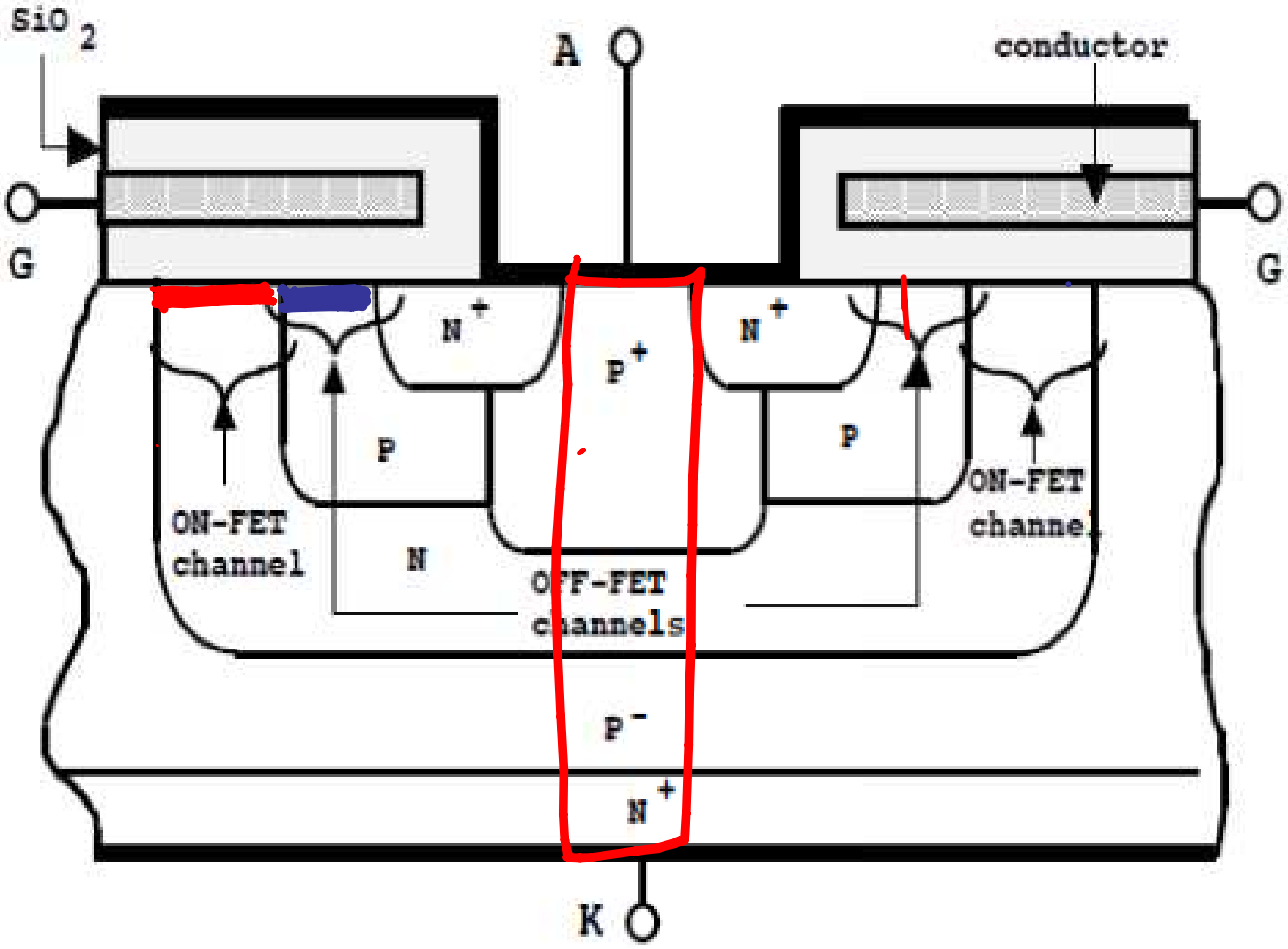
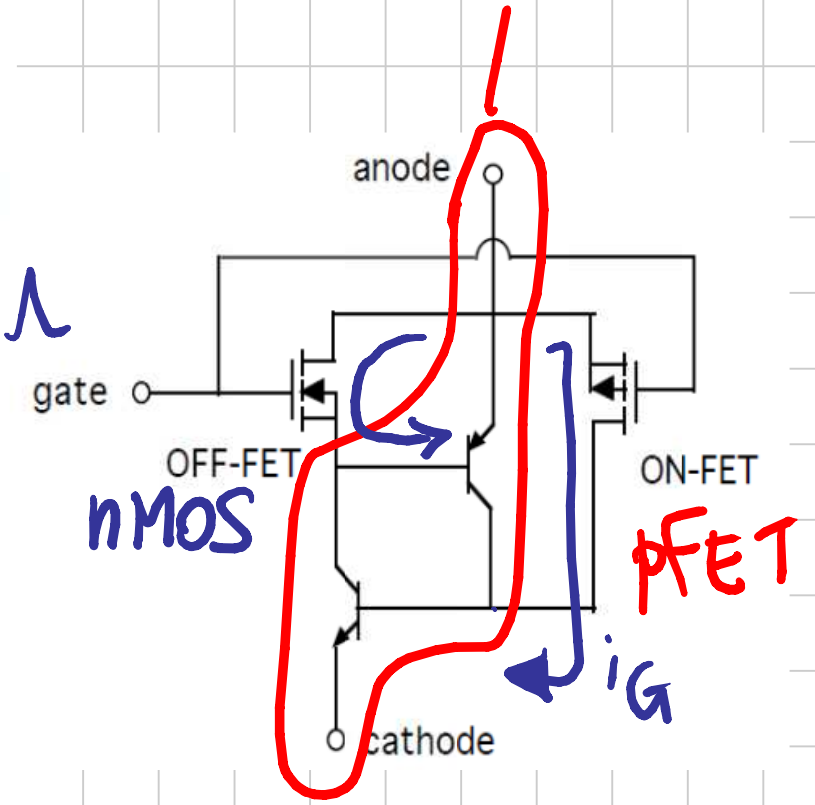
P-MCT - MOS-CONTROLLED THYRISTOR

~10^5 celle in parallelo

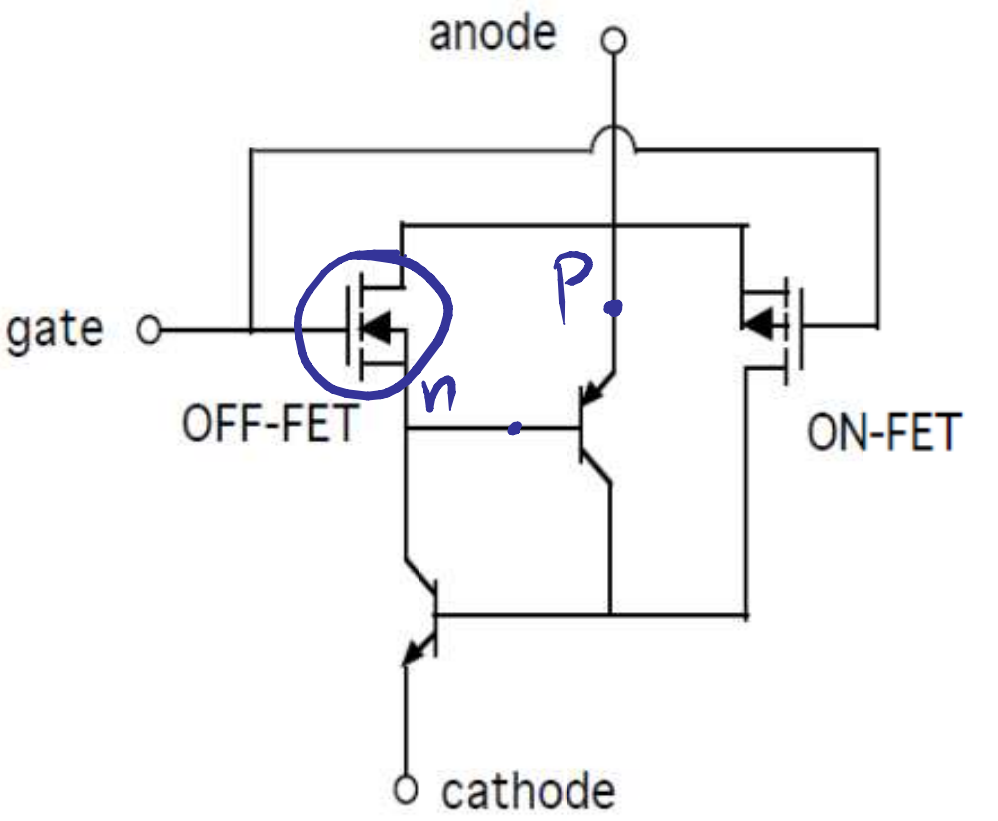
CARATTERISTICA uguale al GTO

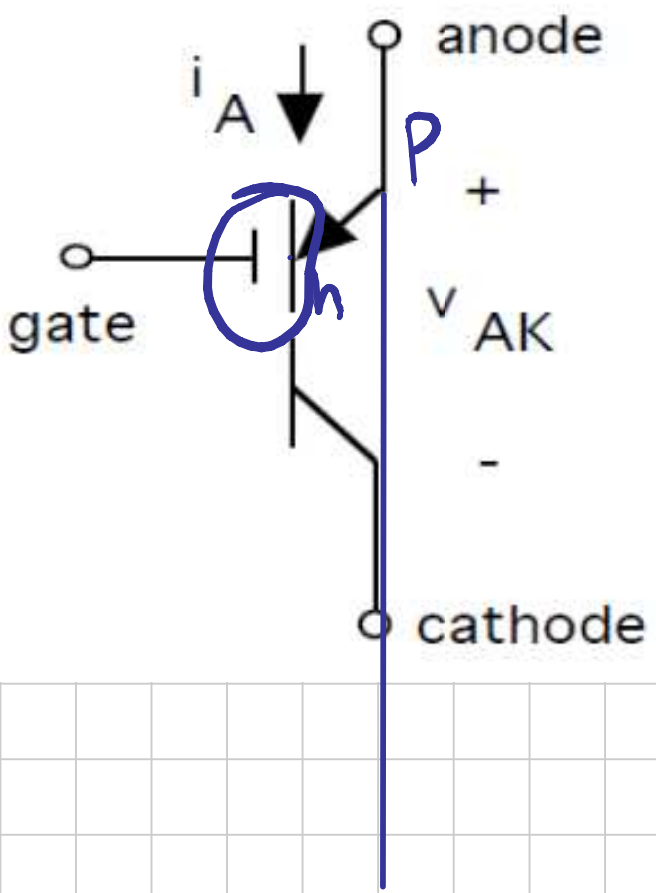


TIRISTORE

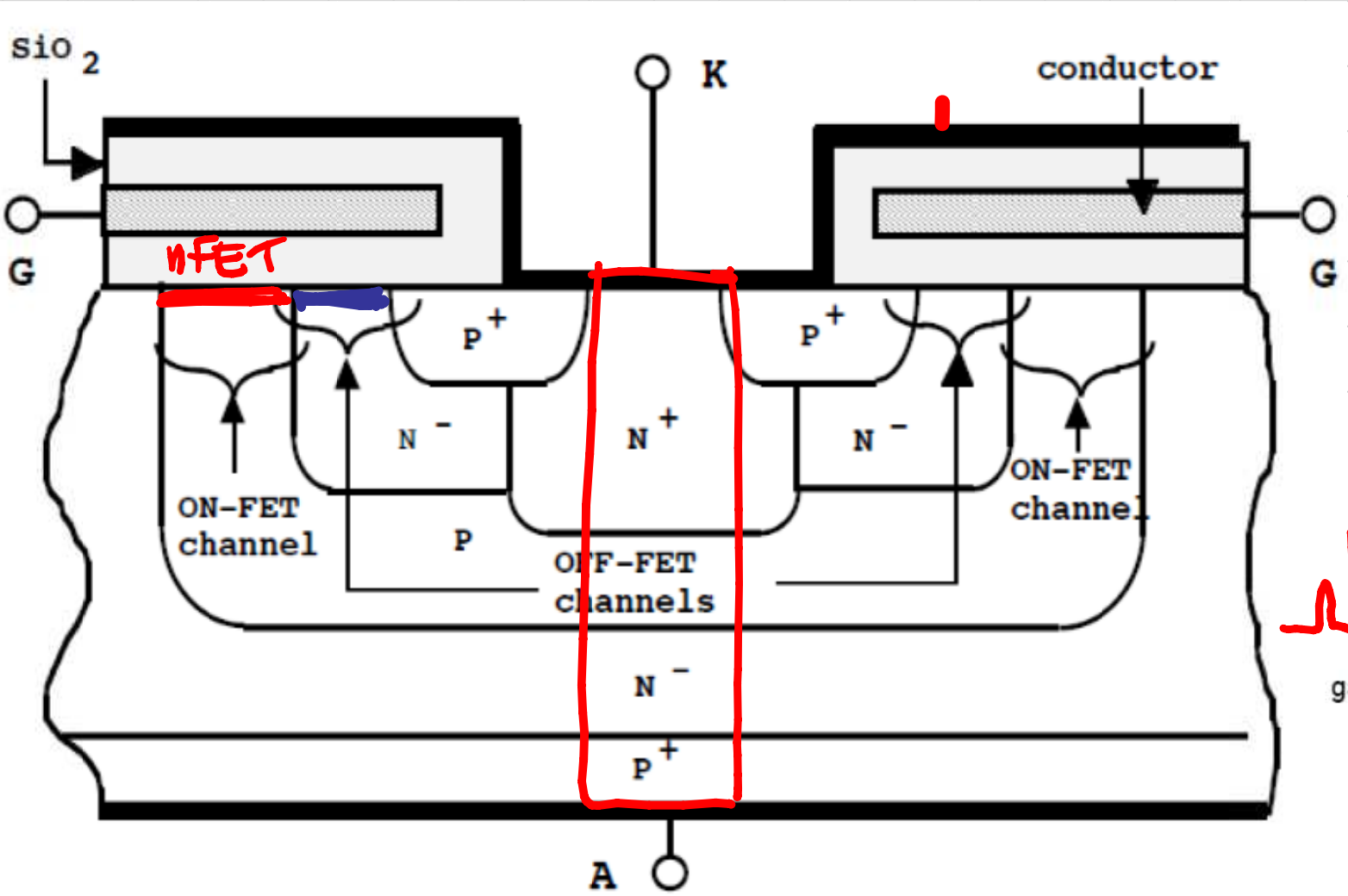


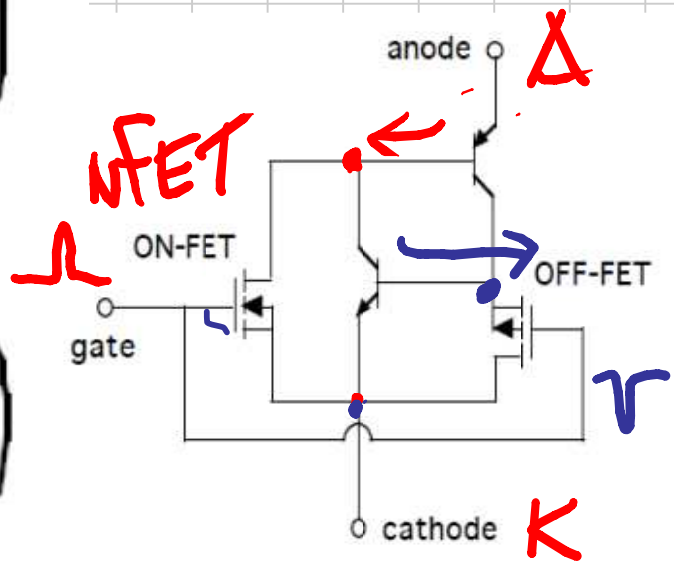
P-MCT


anode
gate
OFF-FET
n
P
ON-FET
cathode

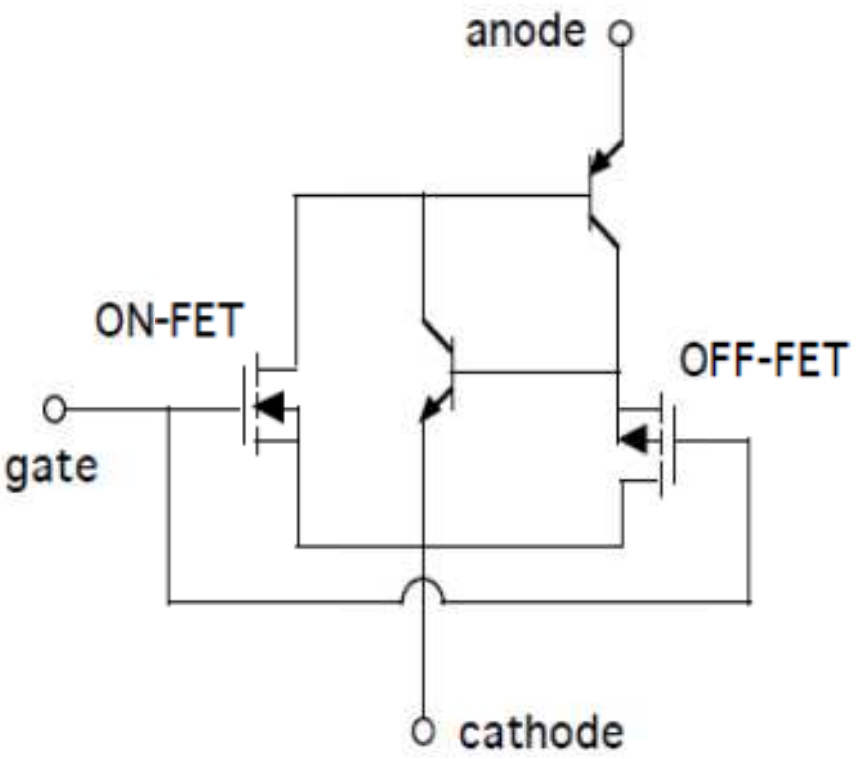

anode
i A
P
+
gate
n
v AK
-
cathode

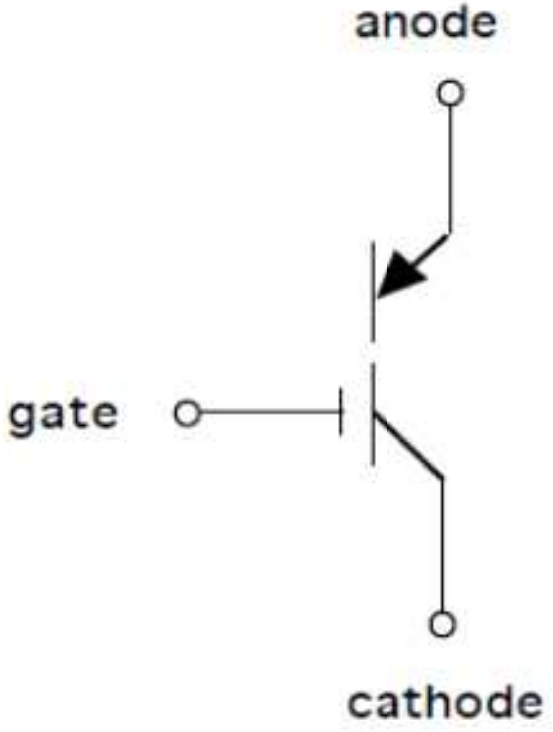
N-MCT

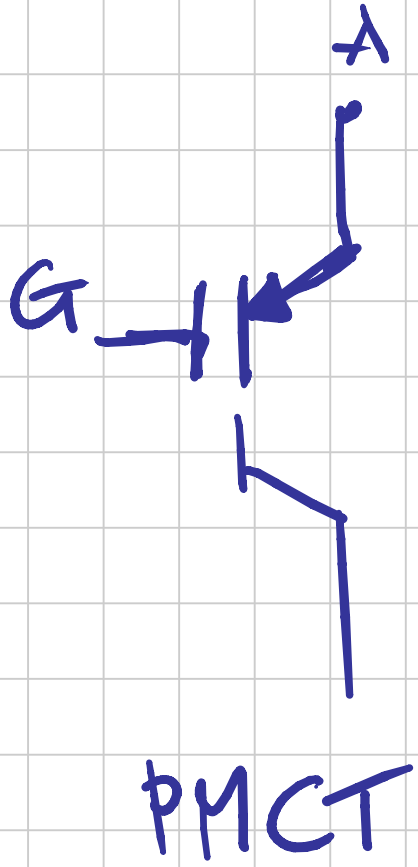

sio 2
K
conductor
G
G
nFET
P+
P+
N-
N+
N-
ON-FET channel
ON-FET channel
P
OFF-FET channels
N-
P+
A

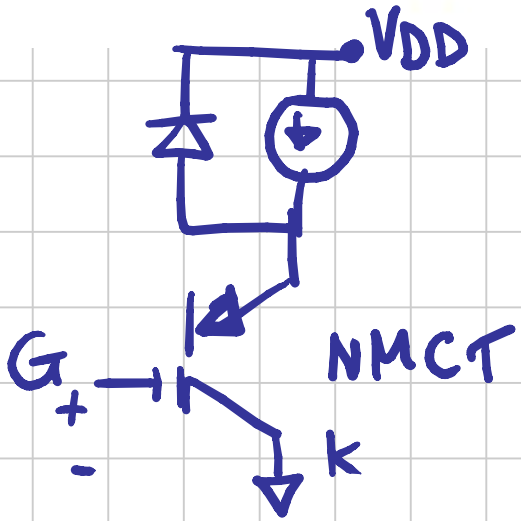

anode
nFET
ON-FET
OFF-FET
gate
cathode
K

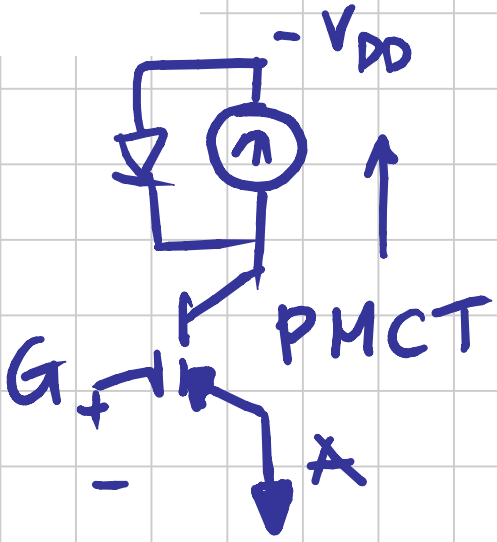
N-MCT


anode
ON-FET
OFF-FET
gate
cathode


anode
gate
cathode

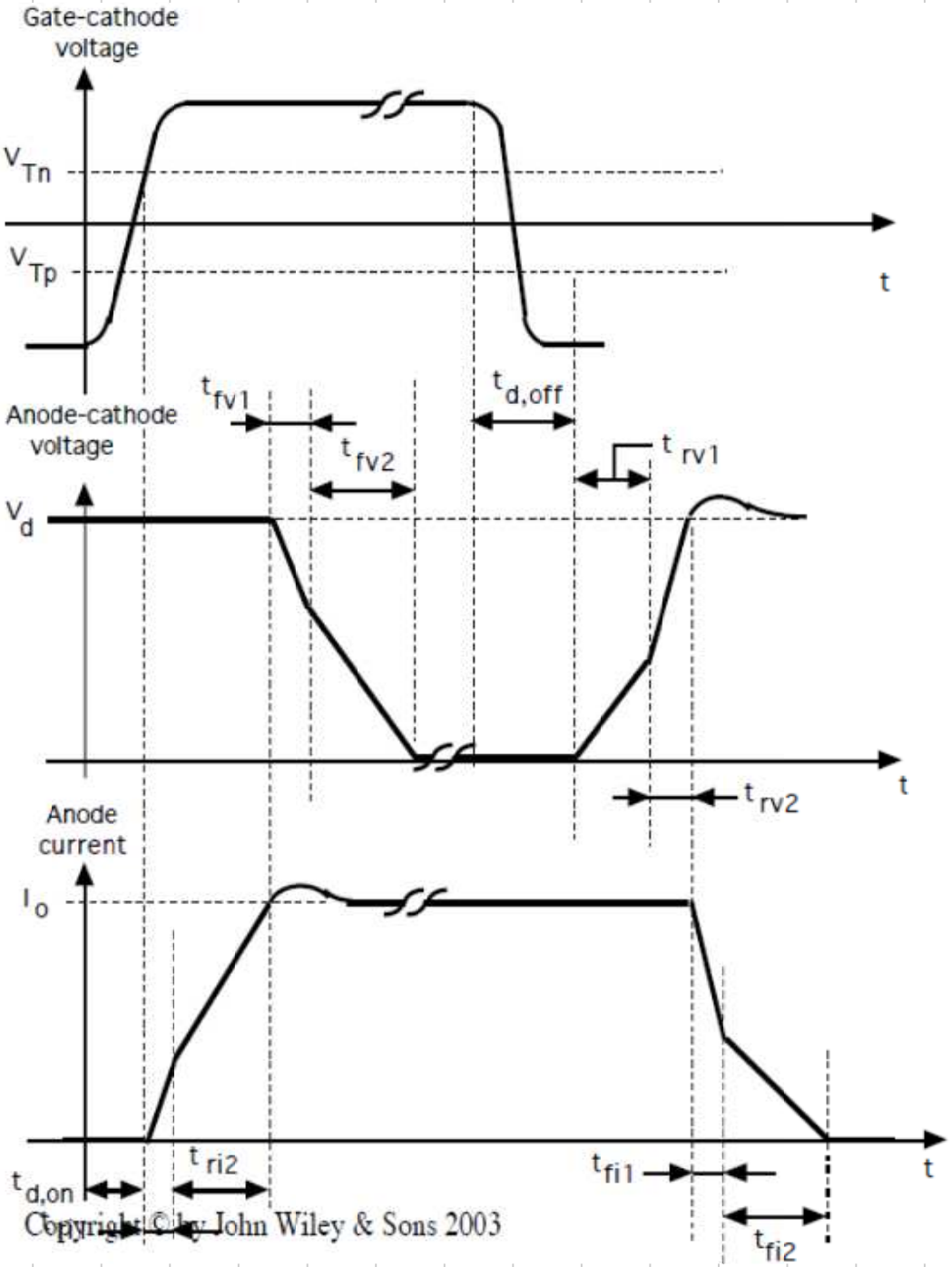

A
G
PMCT

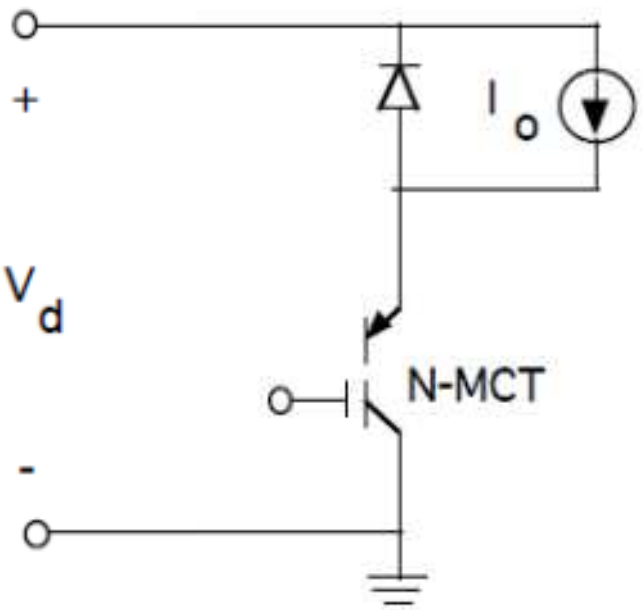

VDD
G
NMCT
k


- VDD
PMCT
G
A

NMCT

COMMUTAZIONE





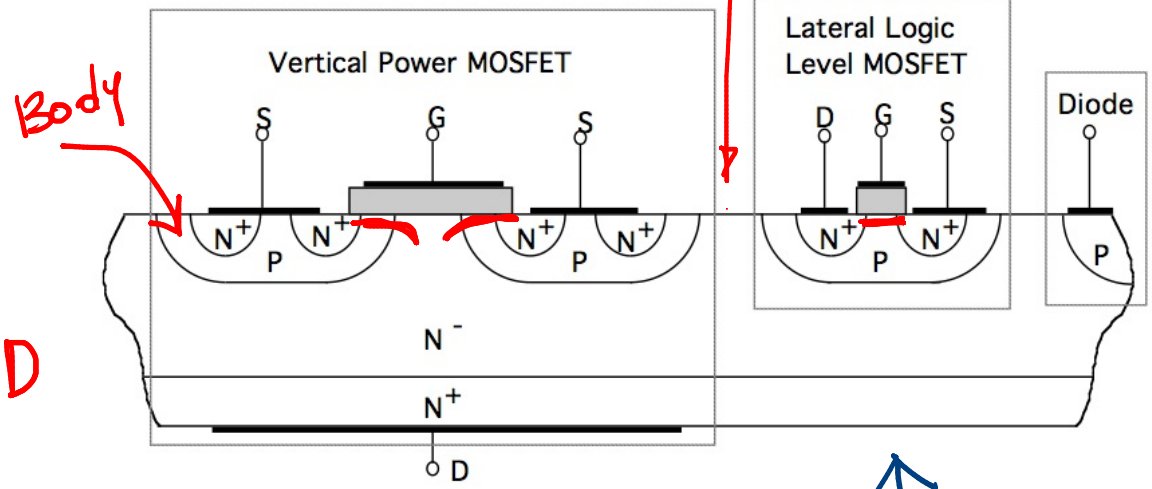
Power IC

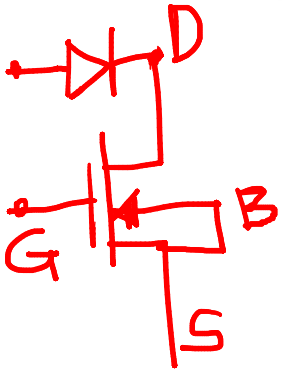
- $I_{max} \sim 50\text{-}100$ A
- $V_{max} < 1000$ V

- Smart switch [con MOSFET, o con BJT]
- HV IC
- discreti

Smart Switch (MOSFET)

tensione alta (drain del MOSFET di potenza)

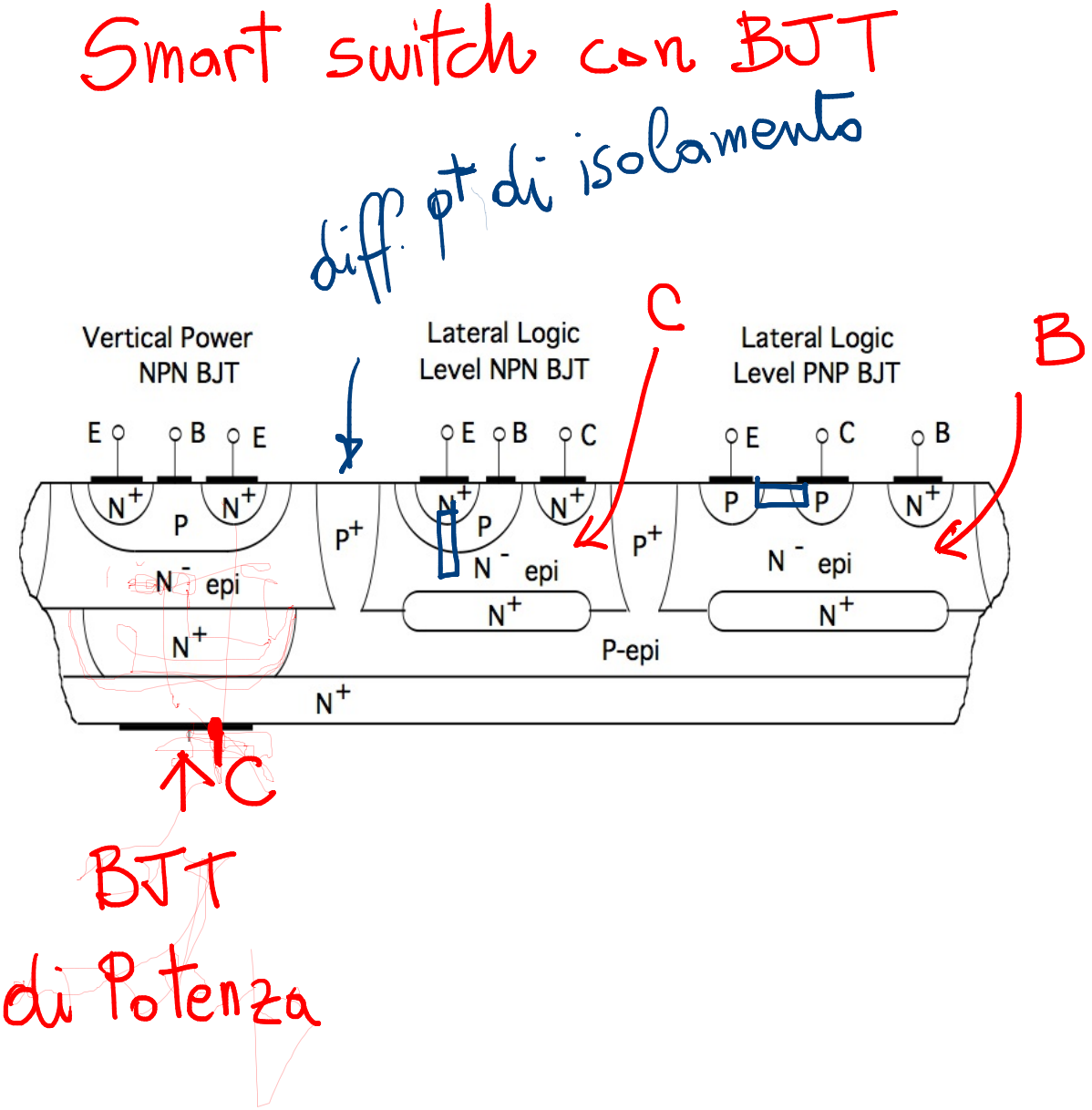




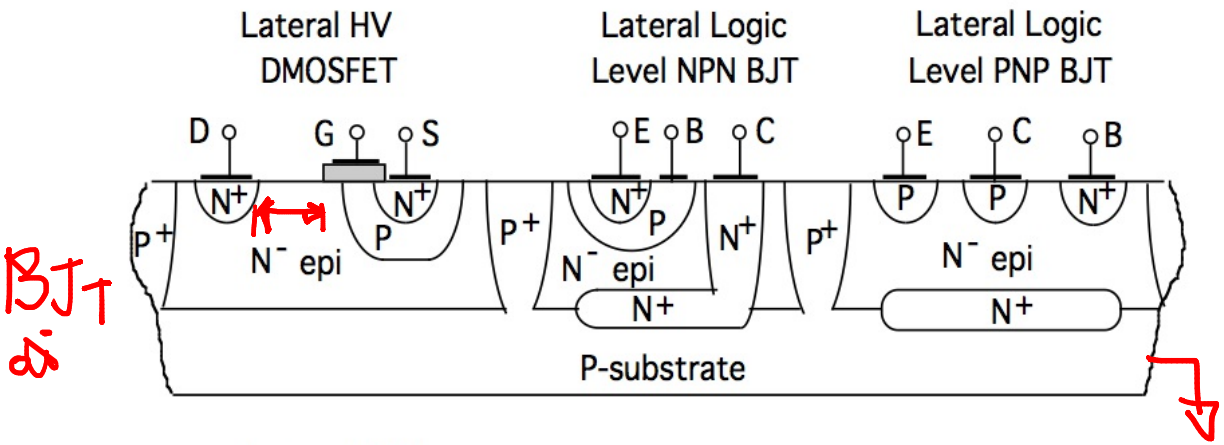
Potenza (MOSFET di Pot)

Logica

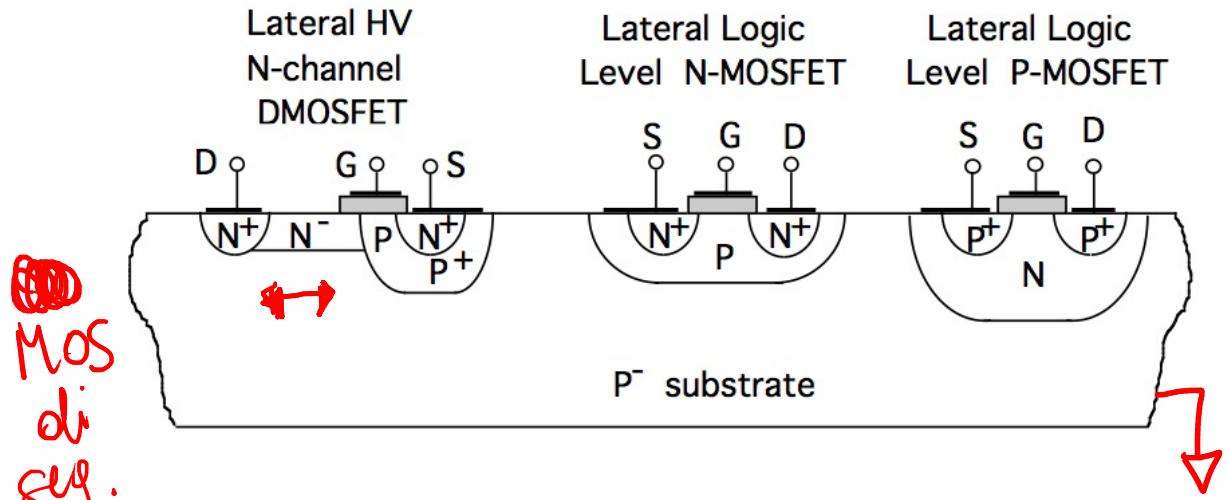
Smart switch con BJT



HV IC



HVIC using junction isolation



HVIC using self-isolation

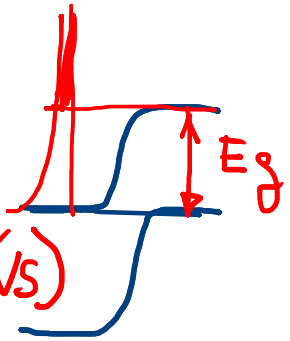
Aspetti critici

- Thermal management [i dispositivi di potenza hanno T più alta]

- Isolamento HV – LV
- Interconnessioni tra i disp di potenza [che passano sopra il circuito LV]

→ Semiconduttori alternativi ←

- GaAs ⌈ gap + alto (1.43eV) → funzion. alte T
  ⌊ mobilità + alta (8000 cm^2/Vs)



SiC → GAP alto [~3eV] → T alte
→ Alta conduttività termica [5 W/cm°C vs 1,5 del Si]
→ Campo elettrico di Breakdown [4×10^6 V/cm , vs 3×10^5 V/cm]

[GaN] → GAP alto [3-4 eV]
→ conduttività termica 1,5 W/cm°C
→ Campo elettrico di Breakdown [4×10^6 V/cm]