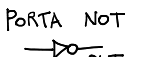
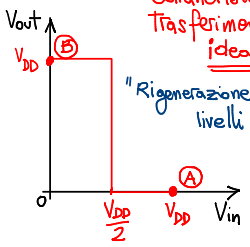
Elettronica Digitale

1 → $V_1 \sim V_{DD}$
0 → $V_0 \sim 0$

PORTA NOT



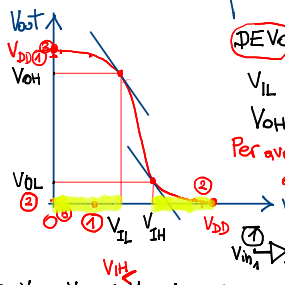
IN	OUT
1	0 → A
0	1 → B



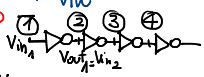
Caratteristica di trasferimento ideale

"Rigenerazione dei livelli logici"

Caratteristica di trasferimento reale

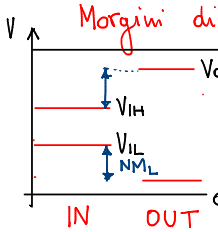


DEVO AVERE
$V_{IL} > V_{OL}$
$V_{OH} > V_{IH}$
Per avere la rigenerazione dei livelli logici



1) Se $0 < V_{in_1} < V_{IL} \rightarrow V_{OH} < V_{out_1} < V_{DD} \rightarrow V_{IH} < V_{in_2} < V_{DD}$
2) Se $V_{IH} < V_{in_1} < V_{DD} \rightarrow 0 < V_{out_1} < V_{OL} \rightarrow 0 < V_{in} < V_{IL}$

Margini di rumore

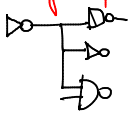


$NM_L \equiv V_{IL} - V_{OL}$
Noise Margin
$NM_H \equiv V_{OH} - V_{IH}$

$NM = \min\{NM_H, NM_L\}$
↑ massima ampiezza del disturbo che non causa errori logici (al max $NM = V_{DD}/2$)

FAN OUT

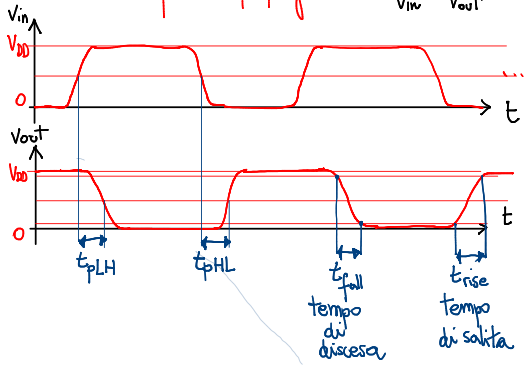
massimo numero di porte che una singola porta logica può pilotare



FAN IN

massimo numero di ingressi che può avere una porta

Tempo di propagazione



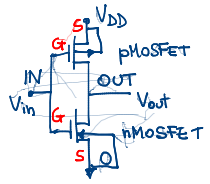
il tempo di propagazione limita la massima frequenza di clock

$$t_{clock} = \frac{1}{f_{clock}} \geq 10\left[t_{pLH} + t_{pHL}\right]$$

Tecnologia CMOS

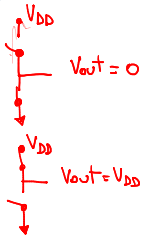
Complementary MOS

inverter



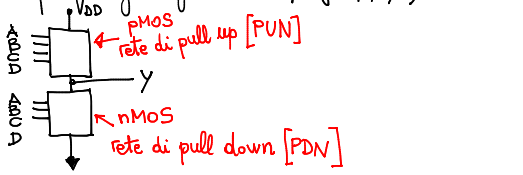
ideale

$V_{in} = V_{DD}$

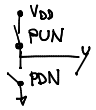


$V_{in} = 0$

porta logica generale $Y = f(A,B,C,D)$

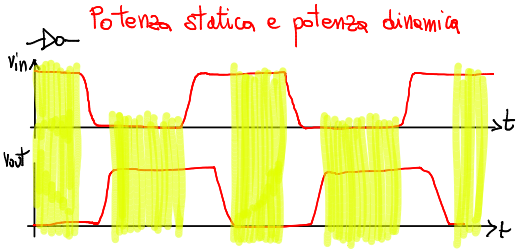


se l'uscita deve essere alta



se l'uscita deve essere bassa

Potenza statica e potenza dinamica

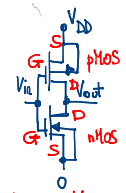


Potenza statica: Potenza dissipata quando i livelli logici sono costanti

Potenza dinamica: Potenza dissipata quando i livelli logici variano

$P_{TOT} = P_S + P_D$

Inverter

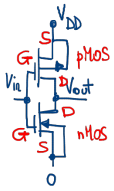


nMOS: $V_{GS_n} < V_{T_n} \rightarrow$ OFF

$V_{in} < V_{Tn} \rightarrow$ OFF

$V_{DS_n} > V_{GS_n} - V_{T_n}$ SAT

$V_{in} > V_{T_n}$ $\begin{cases} V_{out} > V_{in} - V_{T_n} & \text{SAT} \\ V_{out} < V_{in} - V_{T_n} & \text{LIN} \end{cases}$



pMOS

$V_{GS_p} > V_{T_p}$ OFF

$V_{in} - V_{DD} > V_{T_p}$

$V_{in} > V_{T_p} + V_{DD}$ OFF

$V_{in} < V_{T_p} + V_{DD}$ ON

↳ $V_{DS_p} < V_{GS_p} - V_{T_p}$ SAT

$V_{out} - V_{DD} < V_{in} - V_{DD} - V_{T_p}$

$V_{out} < V_{in} - V_{T_p}$ SAT

$V_{out} > V_{in} - V_{T_p}$ LIN

① $0 < V_{in} < V_{T_n}$ $V_{out} = V_{DD}$ NMOS OFF PMOS LIN

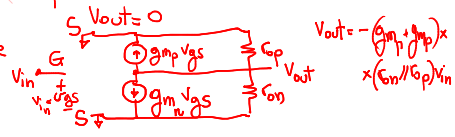
② $V_{out} < V_{DD}$ NMOS SAT - PMOS LIN

③ NMOS SAT PMOS SAT

④ NMOS LIN - PMOS SAT

⑤ $V_{DD} + V_{T_p} < V_{in} < V_{DD}$ NMOS LIN PMOS OFF

piccolo segnale



$V_{out} = -(g_{mp} + g_{mp}) \times (G_{on} // G_{op}) V_{in}$

Valore di Vin quando Vout = VDD/2

siamo nel tratto ③ : PMOS SAT NMOS SAT

NMOS → $I_D = K_n(V_{GS_n} - V_{t_n})^2(1 + \lambda_n V_{DS_n})$ ($V_{GS_n} = V_{in}$, $V_{DS_n} = V_{out}$)

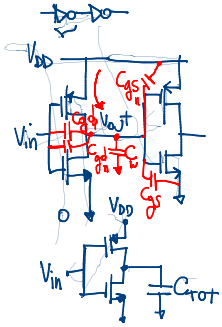
PMOS → $I_D = K_p(V_{GS_p} - V_{t_p})^2(1 + \lambda_p |V_{DS_p}|)$ ($V_{GS_p} = V_{in} - V_{DD}$, $V_{DS_p} = V_{DD} - V_{out}$)

se $V_{out} = \frac{V_{DD}}{2} \rightarrow V_{DS_n} = |V_{DS_p}|$

Se: $\lambda_n = \lambda_p$, $K_N = K_p$, $V_{Tn} = -V_{Tp}$ → INVERTER BILANCIATO o COMPENSATO

allora $V_{in} = \frac{V_{DD}}{2} \rightarrow V_{out} = \frac{V_{DD}}{2}$

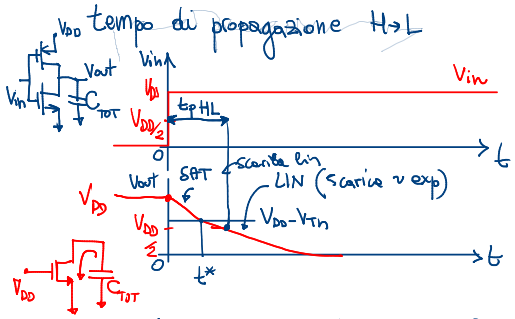
Tempo di propagazione di un inverter CMOS



$C_{TOT} = C_w + C_{gs_n} + C_{gs_p} + 2C_{gd_n} + 2C_{gd_p}$

(la carica richiesta da Cgd ad ogni transizione è 2VddCgd)

tempo di propagazione H→L



$t = 0^+$ $V_{GS} = V_{DD}$ $V_{DS} = V_{DD} > V_{GS} - V_{Tn}$ SAT

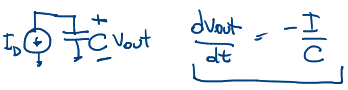
rimane in sat. finché $V_{DS} > V_{GS} - V_{Tn}$

$V_{DS} > V_{DD} - V_{Tn}$

in sat. $I_D = K_n(V_{DD} - V_{Tn})^2$

Costante

scarica a corrente costante

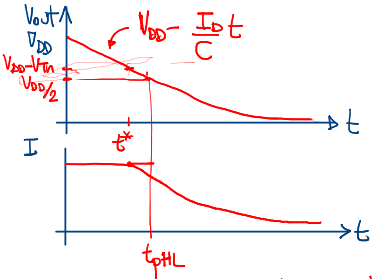


$\frac{dV_{out}}{dt} = -\frac{I}{C}$

se $V_{out} < V_{DD} - V_{Tn}$

il mosfet è in zona lineare

→ scarica ∿ esponenziale



$V_{DD} - \frac{I_D}{C}t$

$\frac{V_{DD}}{2} = V_{DD} - \frac{I_D}{C}t_{pHL} \rightarrow t_{pHL} = \frac{V_{DD}C}{2I_D} = \frac{V_{DD}C}{2K_n(V_{DD} - V_{Tn})^2}$

$t_{pLH} = \frac{V_{DD}C}{2K_p(V_{DD} + V_{Tp})^2}$

se l'inverter è compensato

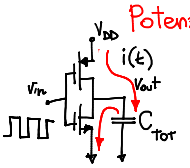
$t_{pHL} = t_{pLH}$

$K_n \uparrow \quad t_p \downarrow$

$\mu \frac{W}{L}\left(\frac{\varepsilon_{ox}}{t_{ox}}\right)$

Sono i fattori principali per la riduzione di t_p

Potenza Dinamica



Carica delle capacità

Vout: da 0V a V_{DD}

$Q = C_{tot} V_{dd}$

Potenza istantanea erogata dall'alim.

$P(t) = V_{dd} i(t)$

integro sul tempo di carica

$\text{Energia} = \int P(t)\,dt = V_{dd} \int i(t)\,dt = C_{tot} V_{dd}^2$

Potenza media erogata dal generatore

$P_D = \frac{\text{Energia}}{T} = f_{clock} C_{tot} V_{dd}^2$

Potenza dinamica dissipata da un circuito integrato

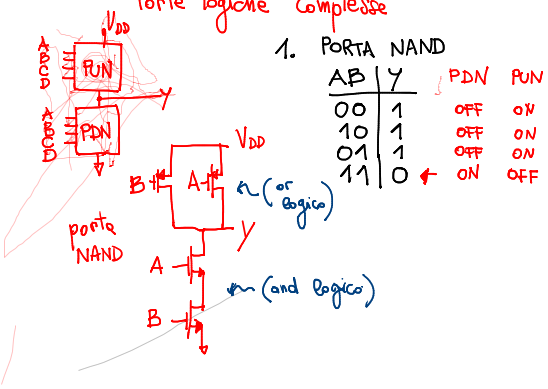
$P_D \simeq \alpha f_{clock} C_{CHIP} V_{dd}^2$

α: fattore di attività

C_{CHIP}: Somma delle capacità di carico di tutto il chip

$P_{TOT} = P_S + P_D$

Porte logiche Complesse

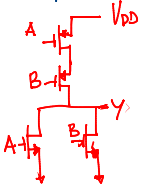


1. PORTA NAND

A	B	Y	PDN	PUN
0	0	1	OFF	ON
1	0	1	OFF	ON
0	1	1	OFF	ON
1	1	0	ON	OFF

2. PORTA NOR

A	B	Y	PDN	PUN
0	0	1	OFF	ON
0	1	0	ON	OFF
1	0	0	ON	OFF
1	1	0	ON	OFF



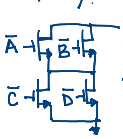
Leggi di de Morgan

$$\begin{cases} \overline{A \cdot B} = \bar{A} + \bar{B} \\ \overline{A + B} = \bar{A} \cdot \bar{B} \end{cases}$$

$Y = 1$ PUN È ON

$\bar{Y} = 1$ PDN È ON

ES $Y = AB + CD \rightarrow \bar{Y} = \overline{AB + CD} = \overline{(AB)} \cdot \overline{(CD)} = (\bar{A} + \bar{B}) \cdot (\bar{C} + \bar{D})$

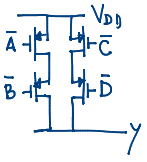


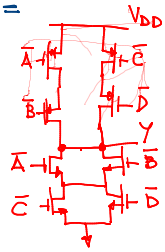
$Y = \bar{\bar{Y}} = \overline{(\bar{A} + \bar{B}) \cdot (\bar{C} + \bar{D})} =$

$= \overline{(\bar{A} + \bar{B})} + \overline{(\bar{C} + \bar{D})} =$

$= A \cdot B + C \cdot D$

PUN

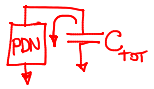


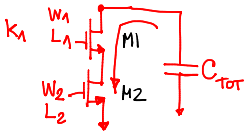


Criterio di dimensionamento

Per ogni porta logica e per ogni configurazione degli ingressi, il tempo di propagazione deve essere uguale o inferiore a quello di un inverter.

tempo di propagazione di una porta logica t_{pHL}





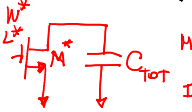
$k_1 = \frac{1}{2}\mu C_{ox}\frac{W_1}{L_1}$

$k_2 = \frac{1}{2}\mu C_{ox}\frac{W_2}{L_2}$

Supponiamo che M1 e M2 siano in zona lineare

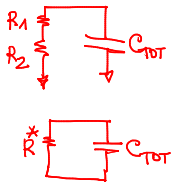
M1 : $I_D = 2K_1(V_{GS_1}-V_t)V_{DS_1} = \frac{V_{DS1}}{R_1}$ $\left[R_1 = \frac{1}{2K_1(V_{GS_1}-V_t)}\right]$

M2 : $I_D = 2K_2(V_{GS_2}-V_t)V_{DS_2} = \frac{V_{DS_2}}{R_2}$ $\left[R_2 = \frac{1}{2K_2(V_{GS_2}-V_t)}\right]$



M^* $I_D = 2K^*(V_{GS}-V_t)V_{DS}$

$I_D = \frac{V_{DS}}{R^*}$ $\left[R^* = \frac{1}{2K^*(V_{GS}-V_t)}\right]$ $V_{DS_1}+V_{DS_2}$



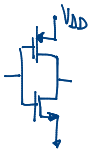
$R^* = R_1 + R_2$

$\frac{1}{K^*} = \frac{1}{K_1} + \frac{1}{K_2}$

$\frac{L^*}{W^*} = \frac{L_1}{W_1} + \frac{L_2}{W_2}$

nel caso in cui $W_1 = W_2 \rightarrow W^* = W_1 = W_2$

$L^* = L_1 + L_2$



$t_{pHL} = \frac{C_{ox}V_{DD}}{2K_n(V_{DD}-V_{T_n})^2}$

$t_{pLH} = \frac{C_{ox}V_{DD}}{2K_p(V_{DD}-V_{T_p})^2}$

→ inverter bilanciato

$V_{T_n} = -V_{T_p}$

$K_n = K_p$ $\rightarrow t_{pHL} = t_{pLH}$

$2\mu_n C_{ox}\left(\frac{W}{L}\right)_n = 2\mu_p C_{ox}\left(\frac{W}{L}\right)_p \rightarrow \mu_n\left(\frac{W}{L}\right)_n = \mu_p\left(\frac{W}{L}\right)_p$

$L = L_{min}$

$\rightarrow \mu_n W_n = \mu_p W_p$

inverter $W_n = W_{min}$

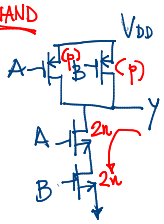
$W_p \cong \frac{\mu_n W_n}{\mu_p}$ per esempio $W_p = 2W_{min}$

$\left(\frac{W_n}{L_n}\right)_n = 2$ ← n: rapporto W/L dell'NMOS dell'inverter

$\left(\frac{W_p}{L_p}\right)_p = 2 \div 6$ ← rapporto W/L del pMOS dell'inverter

per esempio $\frac{5}{3}$

Es NAND



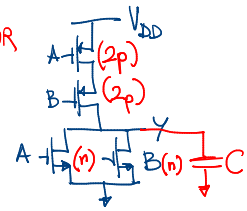
$\left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_B = P$

Occupazione di area ∼ somma delle aree di gate di tutti i transistori

$Area \sim \sum_i W_i L_i = \sum_i \left(\frac{W}{L}\right)_i L_i^2 =$

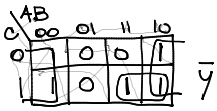
$Area \sim L_{min}^2 \sum_i \left(\frac{W}{L}\right)_i = L_{min}^2 [4n + 2p]$

NOR



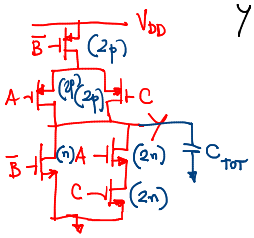
Area $\sim L_{min}^2 (4p+2n)$

$Y = \overline{ABC + \bar{B}}$ $\quad \bar{Y} = ABC + \bar{B}$



$\bar{Y} = \bar{B} + AC$

$Y = \overline{\bar{B} + AC}$



Area $\sim L_{min}^2 [5n+6p]$

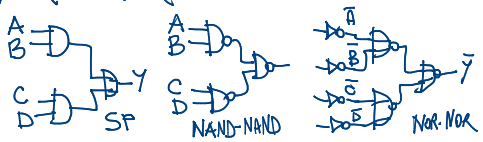
$Y = AB + CD$ ← SP

Qualunque funzione combinatoria si può esprimere come somma di prodotti (SP)

$\bar{Y} = \overline{AB + CD} =$

$Y = \overline{\bar{A}\bar{B}} \cdot \overline{\bar{C}\bar{D}}$ ← NAND-NAND

$\bar{Y} = (\bar{A}+\bar{B}) + (\bar{C}+\bar{D})$ ← NOR-NOR



Area di NAND a 2 input: $L_{min}^2 [4n+2p]$

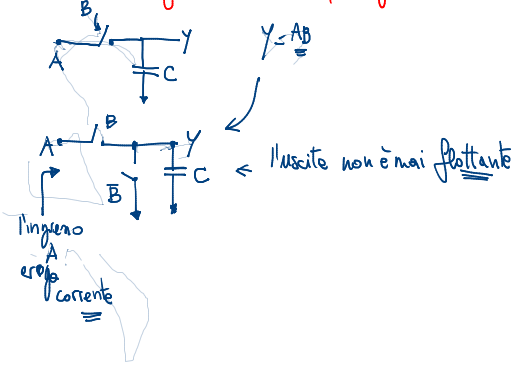
Area di NOR a 2 input: $L_{min}^2 [2n+4p]$

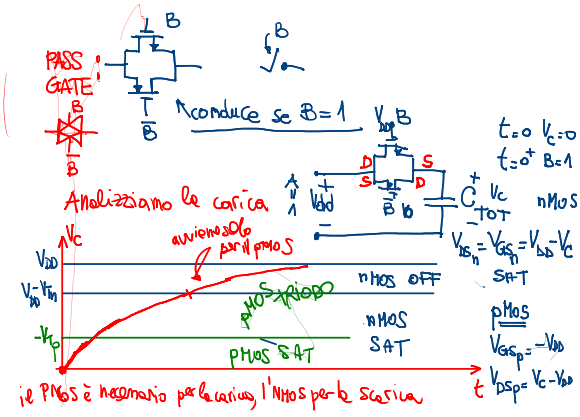
se $n=2$, $p=5$ → NAND: Area $= L_{min}^2 \cdot 18$; NOR Area $= L_{min}^2 \cdot 24$

occupazione d'area minore

NAND-NAND è la forma preferita delle reti combinatorie in tecnologia CMOS

Porte logiche basate su pass gate





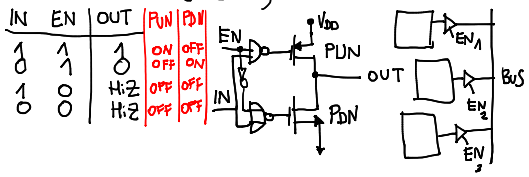
Porte tri-state
3 state (three. state)

USCITA: 1, 0, Hi-Z

↳ uscite in alta impedenza (PUN e PDN aperte)

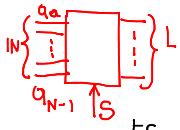
OUT = IN se EN = 1, OUT = Hi-Z se EN = 0

IN	EN	OUT	PUN	PDN
1	1	1	ON	OFF
0	1	0	OFF	ON
1	0	Hi-Z	OFF	OFF
0	0	Hi-Z	OFF	OFF



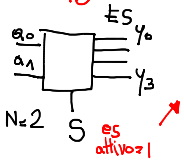
DECODER (decodificatore)

N ingressi · 1 variabile di controllo (Strobe)
· L uscite

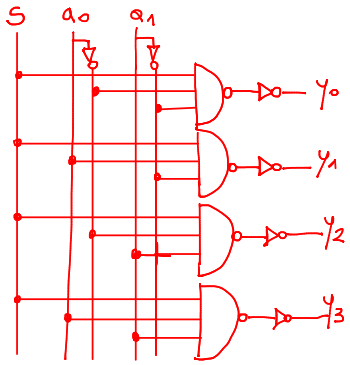


se S = 1 una sola uscita è "attiva" per ogni combinazione degli ingressi

se S = 0 nessuna uscita è attiva



a_0	a_1	S	Y_0	Y_1	Y_2	Y_3
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1
–	–	0	0	0	0	0



n. di transistor
N = 2
L = 4
24 + 12 = 36

in generale
1) L NAND a N+1 ingressi
+
2) L+N inverter

#TR = L(N+1)2 + (L+N)2

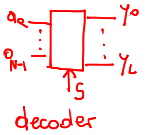
Es: N=4, L=16 → #TR=200

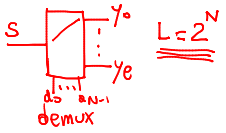
De MUX (Demultiplexer)

1 ingresso, L uscite, N variabili di controllo ($L = 2^N$)

una sola uscita è attiva e riproduce l'ingresso, selezionata in base al valore delle variabili di controllo.

È lo stesso circuito del decoder



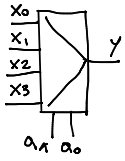


Classificazione dei circuiti in base alla densità di integrazione

N ≈ 10	SSI	Small Scale of Integration
≈ 100	MSI	Medium SI
≈ 10^3	LSI	Large
≈ 10^4–10^8	VLSI	Very Large SI
10^9	GSI	Giga SI

Multiplexer

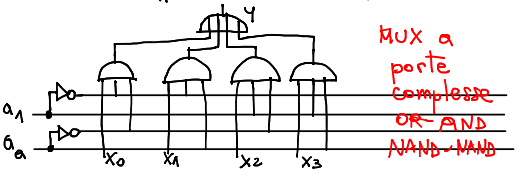
L ingressi, 1 uscita
N variabili di controllo



Es.
N = 2
L = 4

a_1	a_0	Y
0	0	x_0
0	1	x_1
1	0	x_2
1	1	x_3

$Y = \bar{a}_1 \bar{a}_0 x_0 + \bar{a}_1 a_0 x_1 + a_1 \bar{a}_0 x_2 + a_1 a_0 x_3$



MUX a porte complesse
OR-AND
NAND-NAND

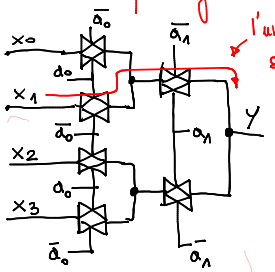
MUX a porte complesse

- L NAND a (N+1) ingressi : $L(N+1)2$ trans.
- 1 NAND a L ingressi : $2L$ trans
- N inverter : $2N$ trans.

TOTALE = $2LN + 4L + 2N$

$L = 16$
$N = 4$ → #trans 200

MUX a pass gate



l'unico percorso che conduce se $a_0 = 1$, $a_1 = 0$ → $Y = X_1$

N variabili di control
$L = 2^N$ ingressi
2^N pass gate +
2^{N-1} pass gate
2^{N-2} " "
..
2

$\#\text{transistori} = 2\sum_{i=1}^{N} 2^i$

Es: $N = 4$ $\#tr = 60$

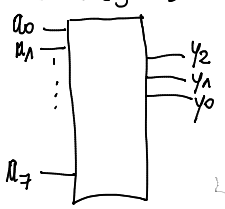
(l'uscita è alimentata direttamente dagli ingressi → + lento)

ENCODER (codificatore)

L ingressi, N uscite $(L \leq 2^N)$

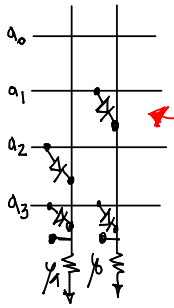
in ogni istante c'è un solo ingresso "attivo". L'uscita è la codifica dell'ingresso attivo

Es: $L = 8$, $N = 3$



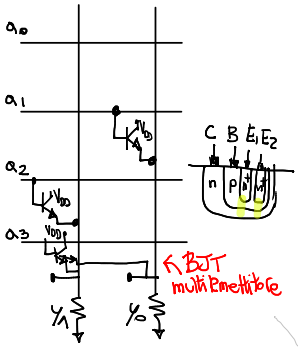
ingresso attivo	$Y_2 Y_1 Y_0$
a_0	000
a_1	001
a_2	010
⋮	⋮
a_7	111

Encoder a diodi $L = 4$, $N = 2$
attivo = alto = 1



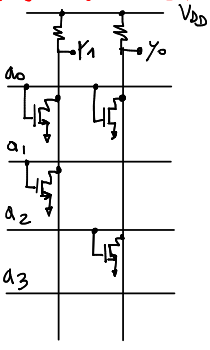
ci vuole un diodo (NON una resistenza)

Encoder a BJT

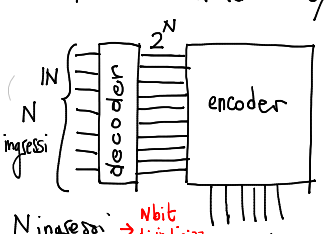


1 BJT multi Emettitore

Encoder a MOSFET



ROM Read Only Memory



N ingressi → N bit di indirizzo
2^N wordline → Num. word da M bit
M uscite → contenuto della word
2^N word de M bit

decoder $N: 2^N$
encoder $2^N : M$

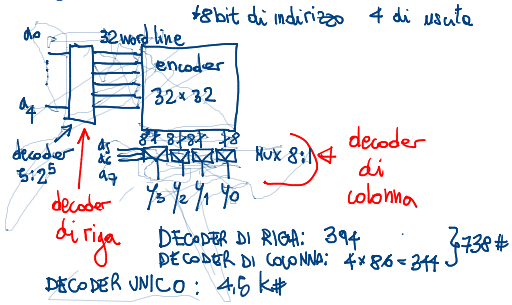
memoria de $2^N \cdot M$ bit

Indirizzamento bidimensionale

encoder quadrato

Es: 1 Kbit ÷ 256 word da 4 bit

8 bit di indirizzo 4 di uscita



DECODER DI RIGA: 394
DECODER DI COLONNA: 4 × 86 = 344 } 738 #

DECODER UNICO: 4,6 k#

→ ROM ←

↓

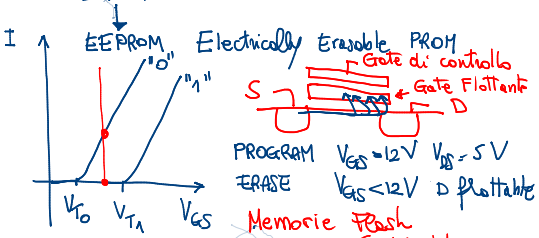
PROM Programmable ROM

↓

EPROM Erasable

↓

EEPROM Electrically Erasable PROM



PROGRAM $V_{GS} = 12\,V$ $V_{DS} = 5\,V$

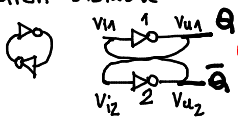
ERASE $V_{GS} < 12\,V$ D flottante

Memorie Flash

1 Transistore (2 gate) x bit

Reti sequenziali

Latch bistabile 2 stati stabili



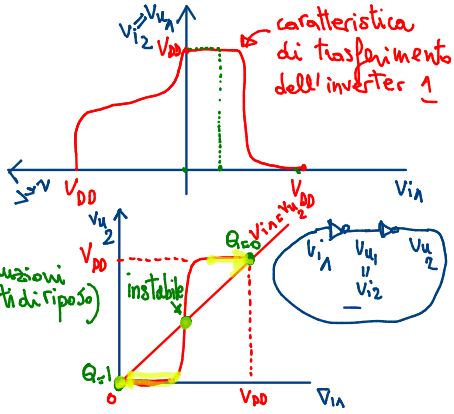
① $V_{i1} = V_{u2} = 0$ $Q = 1$ $V_{u1} = V_{i2} = V_{DD}$

② $V_{i2} = V_{u1} = 0$ $Q = 0$ $V_{u2} = V_{i1} = V_{DD}$

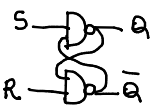
$V_{u2} = V_{u2}(V_{i2}) =$

$V_{i2} = V_{u1}(V_{i1})$

$V_{u2} = V_{u2}(V_{u1}(V_{in}))$



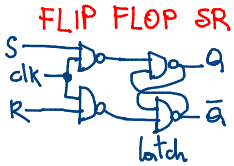
latch SR



se $S=1$, $R=1$ il latch conserva lo stato stabile

SR	Q $\bar{Q}$
11	conserva lo stato stabile $Q=1$ $\bar{Q}=0$, $Q=0$ $\bar{Q}=1$
10	0 1
01	1 0
00	1 1 ← NON è consentito perché non è uno stato stabile

FLIP FLOP SR



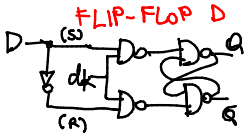
se clk = 0 il latch conserva lo stato

se clk = 1

S_n	R_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	non determinato

SR	
00	latch conserva
10	$Q=1$ $(\bar{Q}=0)$
01	$Q=0$ $(\bar{Q}=1)$
11	Non è consentita

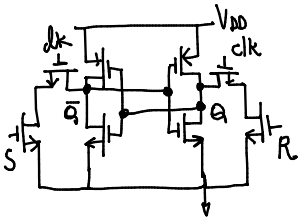
FLIP-FLOP D



D_n	Q_{n+1}
0	0
1	1

Registro a 1 bit

FLIP. FLOP SR a 8 transistori



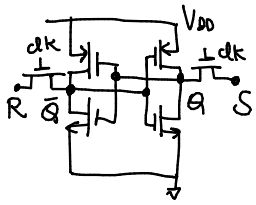
se clk = 0
il latch è isolato
(conserva lo stato)

se clk = 1

S	R	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	non det.

S	R	Q $\bar{Q}$
1	0	1 0
0	1	0 1
0	0	conserva lo stato
1	1	non consentita (Q indeterm.)

FLIP FLOP SR a 6 transistori



S_n	R_n	Q_{n+1}
1	0	1
0	1	0
1	1	—
0	0	—

RAM

Random Access Memory

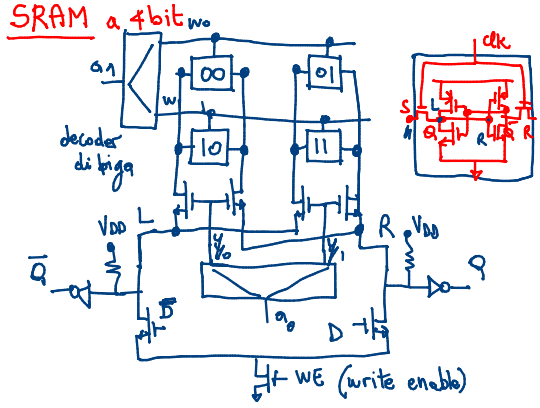
- SRAM — Static RAM
- DRAM — Dynamic RAM

SRAM
+ più veloce

DRAM
+ minor costo [densità + alta]
+ minor consumo

in un PC → Cache, Memoria

SRAM a 4 bit



LETTURA — WE = 0

L = Q del latch che ho indirizzato con (a_1, a_0)
R = $\bar{Q}$

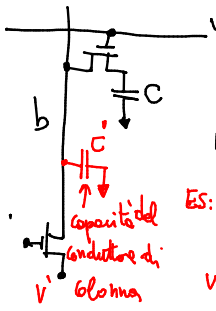
SCRITTURA — WE = 1

D = 1 → $\bar{Q}$ = 0, Q = 1 | del latch che ho indirizzato con (a_1, a_0)

D = 0 → $\bar{Q}$ = 1, Q = 0 |

DRAM

Cella di memoria = 1 transistore + 1 capacità



informazione codificata nella carica della capacità

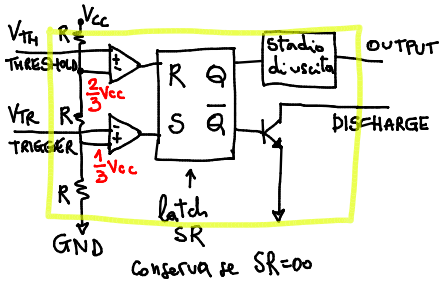
↳ C'è bisogno di un REFRESH ogni 1/10 ms

ES: su C di sia V_{DD}

$Q = CV_{DD} = (C+C')V'$

$V' = \frac{C}{C+C'} V_{DD} \ll V_{DD}$ ha bisogno di un amplificatore

TIMER LM555



Conserva se SR=00

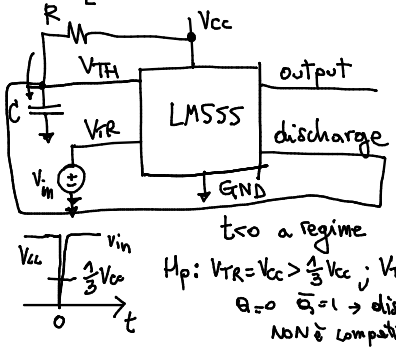
1) $V_{TH} > \frac{2}{3}V_{cc}$, $V_{TR} > \frac{1}{3}V_{cc}$ → RS=10 → OUTPUT=0, DISCHARGE=GND

2) $V_{TH} > \frac{2}{3}V_{cc}$, $V_{TR} < \frac{1}{3}V_{cc}$ → RS=11 → da non utilizzare (lo stato del latch non può essere conservato)

3) $V_{TH} < \frac{2}{3}V_{cc}$, $V_{TR} > \frac{1}{3}V_{cc}$ → RS=00 → OUTPUT e DISCHARGE non variano

4) $V_{TH} < \frac{2}{3}V_{cc}$, $V_{TR} < \frac{1}{3}V_{cc}$ → RS=01 → output=1, DISCHARGE=Hi-Z

Generatore di impulso rettangolare [multivibratore monostabile]



t<0 a regime

Hp: $V_{TR} = V_{cc} > \frac{1}{3}V_{cc}$; $V_{TH} = V_{cc} > \frac{2}{3}V_{cc}$

Q=0 $\bar{Q}$=1 → discharge, gnd

NON è compatibile con Hp.

Hp $V_{TR} = V_{cc} > \frac{1}{3}V_{cc}$ $V_{TH} = 0 < \frac{2}{3}V_{cc}$

SR=00 output=0 discharge, gnd

$t<0^-$

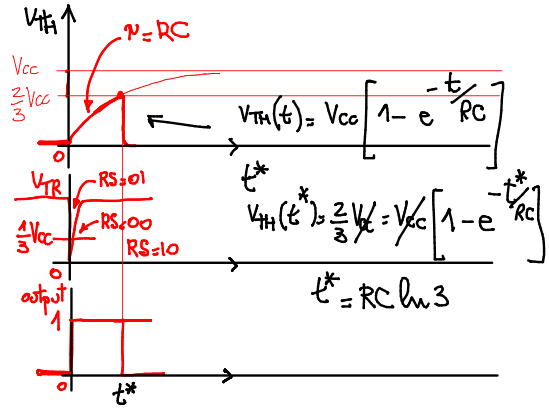
t_0^+ $V_{TR} < \frac{1}{3}V_{cc}$ $V_{TH} = 0 < \frac{2}{3}V_{cc}$

RS=01 → output=1, discharge → hi-Z

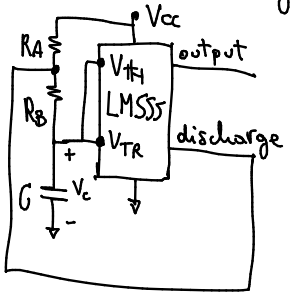
la capacità si carica con costante di tempo RC e asintoto V_{cc}

→ quando V_{TR} supera $\frac{1}{3}V_{cc}$ NON cambia niente (il latch conserva lo stato)

t t^* $V_{TH} \geq \frac{2}{3}V_{cc}$ $V_{TR} > \frac{1}{3}V_{cc}$ → RS=10, output=0, discharge → gnd



Generatore d'onda rettangolare [multivibratore bistabile]



$V_{TH} = V_{TR}$

se $V_c > \frac{2}{3}V_{cc}$ output 0 (discharge=gnd)

se $\frac{1}{3}V_{cc} < V_c < \frac{2}{3}V_{cc}$ output cost.

$V_c < \frac{1}{3}V_{cc}$ output 1 (discharge=hiZ)

$t=0$ $V_c=0$ output=1 discharge=hiZ

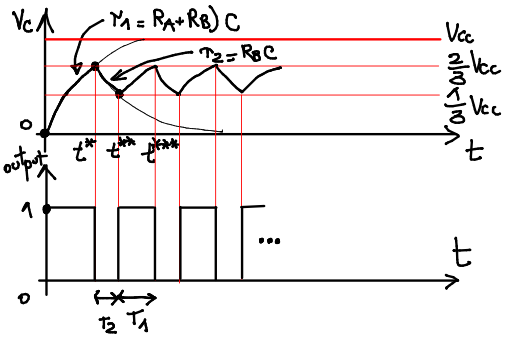
C si carica con costante di tempo $\tau_1 = (R_A+R_B)C$ e asintoto V_{cc}

a) quando $V_c = \frac{2}{3}V_{cc}$ → output = 0 discharge = gnd

C di scarica con costante di tempo $\tau_2 = R_B C$ e asintoto 0 V

b) quando $V_c = \frac{1}{3}V_{cc}$ → output = 1 discharge = hiZ

C si carica con costante di tempo τ_1 e asintoto V_{cc}



T_2: $t^* < t < t^{**}$

$V_c(t) = Ae^{-t/\tau_2} + B$

$V_c(t^*) = \frac{2}{3}V_{cc} = Ae^{-t^*/\tau_2} + B$

$\lim_{t\to\infty} V_c = 0 \rightarrow B = 0$ $\quad A = \frac{2}{3}V_{cc}e^{t^*/\tau_2}$

$\frac{1}{3}V_{cc} = V_c(t^{**}) = \frac{2}{3}V_{cc}e^{-T_2/\tau_2} \rightarrow T_2 = \tau_2 \ln 2$

$T_2 = R_B C \ln 2$

T_1 $t^{**} < t < t^{***}$

$V_c(t) = Ae^{-t/\tau_1} + B$

$V_c(t^{**}) = \frac{1}{3}V_{cc} = Ae^{-t^{**}/\tau_1} + B$

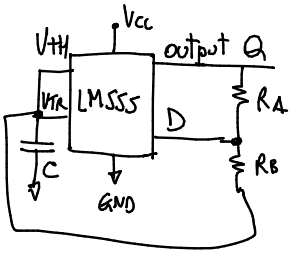
$\lim_{t\to\infty} V_c(t) = V_{cc} = B$ $\quad A = -\frac{2}{3}V_{cc}e^{t^{**}/\tau_1}$

$\frac{2}{3}V_{cc} = V_c(t^{***}) = -\frac{2}{3}V_{cc}e^{-T_1/\tau_1} + V_{cc}$

$T_1 = \tau_1 \ln 2 = (R_A+R_B)C \ln 2$

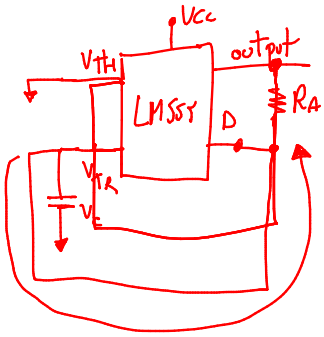
$\rightarrow T = T_1 + T_2 = (\tau_1+\tau_2)\ln 2 = (2R_B+R_A)C \ln 2$

$\delta = \frac{T_1}{T_1+T_2} = \frac{\tau_1}{\tau_1+\tau_2} = \frac{R_B}{2R_B+R_A}$



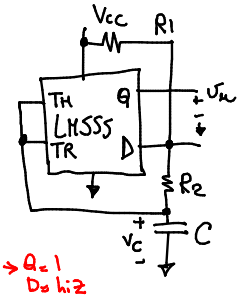
?

Stesso comportamento del circuito precedente



$t=0$
$v_C=0$
output = 1
D = hiZ
C si carica con $\tau = R_A C$
a risistore V_{cc}

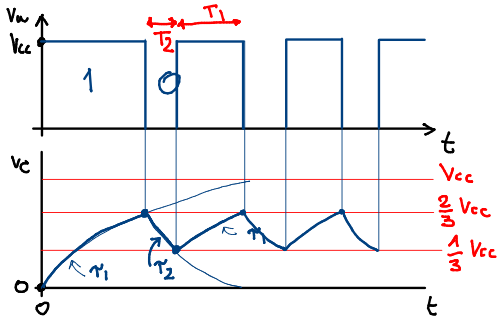
Es. 28/1/2010 n. 3



$R_1 = 5\,k\Omega$
$R_2 = 15\,k\Omega$
$C = 1\,\mu F$

- $v_c < \frac{1}{3}V_{cc} \rightarrow Q=1$, D = hiZ
- $v_c > \frac{2}{3}V_{cc} \rightarrow Q=0$, $D \rightarrow$ gnd
- $\frac{1}{3} < v_C < \frac{2}{3}V_{cc} \rightarrow$ conservazione dello stato

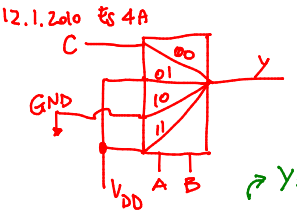
carica $\tau_1 = (R_1+R_2)C$
scarica $\tau_2 = R_2 C$

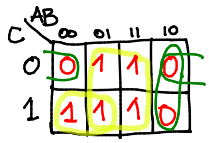


$t=0$, $v_C=0 \rightarrow Q=1$, $D=$ GND $\rightarrow$ carica con τ_1

$T_1 = \tau_1 \ln 2 \overset{1.39ms}{\sim}$ $T_2 = \tau_2 \ln 2 = 10.4\,ms$ $T = T_1 + T_2 = 24.3\,ms$

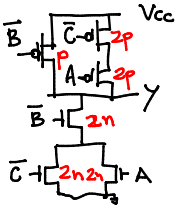
12.1.2010 Es 4A



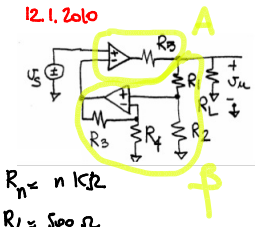


$Y = B + C\bar{A}$

$[\bar{Y} = A\bar{B} + \bar{C}\bar{B}]$



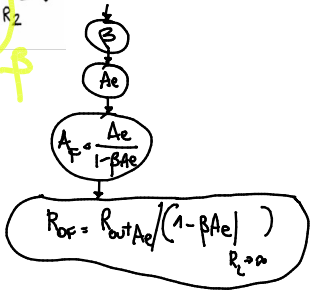
12.1.2010

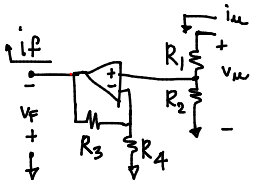


$R_n = n\,k\Omega$
$R_L = 500\,\Omega$
$A_V = 1000$

? fdT e R_{OF}

Prelievo di tensione
Inserzione di Tensione





(B)

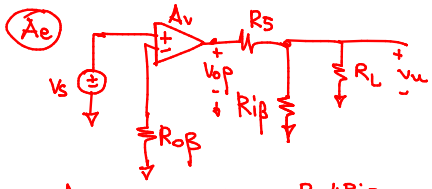
$v_f = \beta v_M + R_{O\beta} i_f$

$i_M = \frac{v_M}{R_{i\beta}} + \cancel{i_f}$

$\beta = \frac{v_f}{v_M}\Big|_{i_f=0} = -\left(1+\frac{R_3}{R_4}\right)\cdot\frac{R_2}{R_2+R_1} = -\frac{7}{4}\cdot\frac{1}{3} = -\frac{7}{6} \simeq -1.17$

$R_{O\beta} = \frac{v_f}{i_f}\Big|_{v_M=0} \simeq 0$ (ccv)

$R_{i\beta} = \frac{v_M}{i_M}\Big|_{i_f=0} = R_1 + R_2 \simeq 3\,k\Omega$



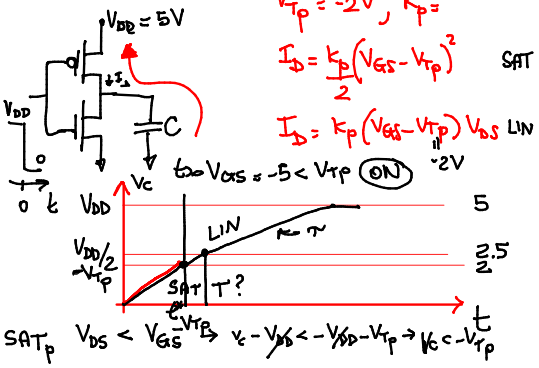
$V_{op} = A_V V_S$ $\quad V_u = V_{op} \cdot \frac{R_L /\!/ Ri\beta}{R_S + R_L /\!/ Ri\beta}$

$A_e = \left.\frac{V_u}{V_S}\right|_{\beta=0} = A_V \frac{R_L /\!/ Ri\beta}{R_S + R_L /\!/ Ri\beta} = 1000 \frac{500 /\!/ 3000}{5000 + 500 /\!/ 3000} = 78.85$

$A_F = \frac{A_e}{1 - \beta A_e} = 0.85$ $\quad (-1.17)$

$R_{OF} = \frac{R_S /\!/ Ri\beta}{1 - \beta A_e|_{R_L \to \infty}} = \frac{R_S /\!/ Ri\beta}{1 - \beta A_V \frac{Ri\beta}{R_S + Ri\beta}} \simeq \frac{R_S}{-\beta A_V} = 4.28\,\Omega$

30.6.2010 Es. 2.



$V_{Tp} = -2V$, $K_p =$

$I_D = \frac{K_p}{2}(V_{GS} - V_{Tp})^2$ SAT

$I_D = K_p (V_{GS} - V_{Tp}) V_{DS}$ LIN

$t = 0 \Rightarrow V_{GS} = -5 < V_{Tp}$ (ON)

SAT$_p$ $V_{DS} < V_{GS} - V_{Tp} \Rightarrow v_c - V_{DD} < -V_{DD} - V_{Tp} \Rightarrow V_c < -V_{Tp}$

SAT $\quad I_D = \frac{K_{Tp}}{2}(V_{GS} - V_{Tp})^2 = \frac{2 \cdot 10^{-3}}{2} \cdot (5-2)^2 = 9\,mA$

$\frac{dV_c}{dt} = \frac{I_D}{C} \Rightarrow v_c(t) = \frac{I_D t}{C} = \frac{9 \cdot 10^{-3}}{1 \cdot 10^{-9}} \cdot t =$

$V_c = 9 \cdot 10^6 t$

$V_c(t^*) = \frac{V_{DD}}{2} \Rightarrow t^* = \frac{C}{I_D}\frac{V_{DD}}{2} = \frac{10^{-9}}{9 \cdot 10^{-3}} \cdot \frac{5}{2} = 0.28\,\mu s$

$t > t^*$ → MOSFET in zona lineare

$I_D = K_p (V_{GS} - V_{Tp}) V_{DS} \Rightarrow R_{eq} = \frac{1}{K_p |V_{GS} - V_{Tp}|} =$

$= \frac{1}{2 \cdot 10^{-3} \cdot 3} = 167\,\Omega$

$t > t^*$

$v_c(t) = Ae^{-t/\tau} + B$ $\quad \tau = R_{eq} C = 0.167\,\mu s$

$v_c(t^*) = 2V$

$\lim_{t \to \infty} v_c(t) = V_{DD} = 5V = B$

$v_c(t^*) = 2V = Ae^{-t^*/\tau} + V_{DD} \Rightarrow A = (-V_{Tp} - V_{DD}) e^{t^*/\tau}$

$-V_{Tp}$

$v_c(T) = \frac{V_{DD}}{2} \geq Ae^{-T/\tau} + B$

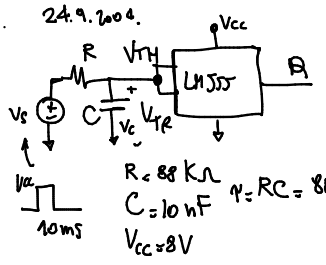
$?$

$\frac{V_{DD}}{2} = \left[-V_{Tp} - V_{DD}\right] e^{-\frac{T - t^*}{\tau}} + V_{DD} \Rightarrow T = t^* + \tau \ln\left(\frac{V_{DD} + V_{Tp}}{V_{DD}/2}\right)$

$= 0.28\,\mu s + 0.167 \ln 1.2$

$= 0.31\,\mu s$

24.9.2004.

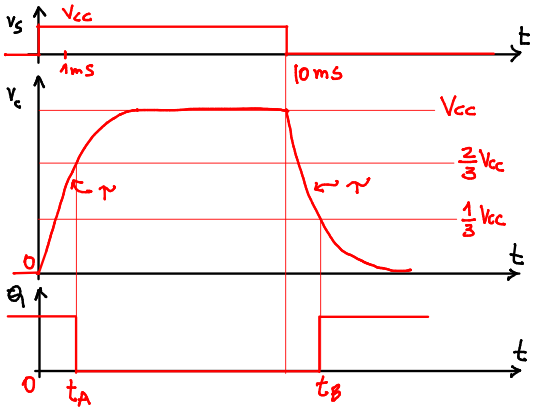


$R < 88\,K\Omega$

$C = 10\,nF$

$V_{CC} = 8V$

$\tau = RC = 880\,\mu s = 0.88\,ms$



$t>0$ $\quad v_c(t) = V_{cc}\left[1-e^{-t/\tau}\right]$

$v_c(t_A) = \frac{2}{3}V_{cc} = V_{cc}\left[1-e^{-t_A/\tau}\right]$

$t_A = \tau \ln 3 = 0.88 \ln 3 \simeq 0.97\,ms$

$t>10ms$ $\quad v_c(t) = V_{cc}\,e^{-(t-T)/\tau}$ $\quad T=10ms$

$v_c(t_B) = \frac{1}{3}V_{cc} = V_{cc}\,e^{-(t_B-T)/\tau}$

$t_B = T + \tau \ln 3 = 10 + 0.88 \ln 3 \simeq 10.97\,ms$