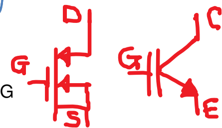
IGBT
Insulated-Gate Bipolar Transistor

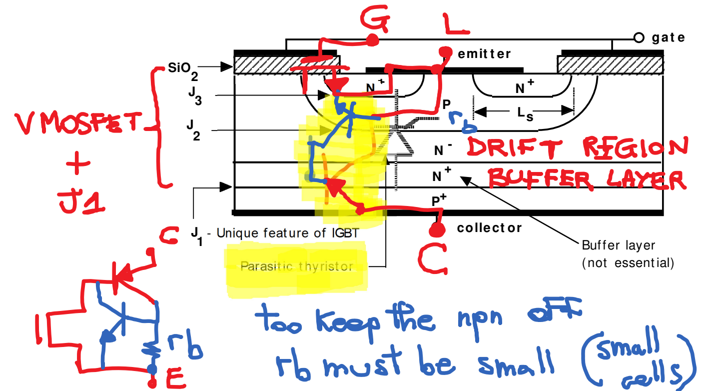
	PRO	CON
MOSFET	Fast Turn Off	High V_{ON} (no conductance modulation)
BJT	Low V_{ON} (conductance modulation)	Slow Turn Off

IGBT

MOSFET with added junction between D and G to introduce conductance modulation



IGBT



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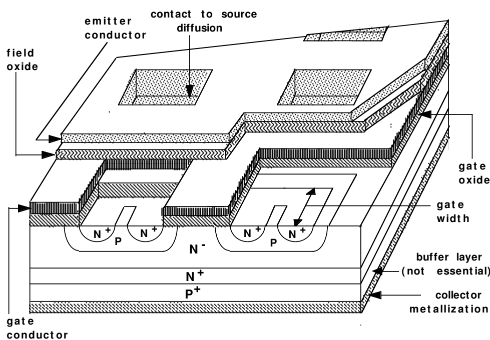
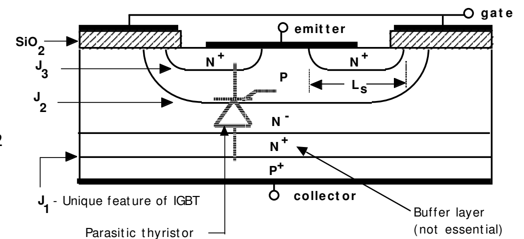


Blocking state

MOSFET is **OFF**

If $V_{CE} > 0$
Voltage is sustained by J_2

If $V_{CE} < 0$
Voltage is sustained by J_1 and J_3



The buffer layer allows punchthrough:

- If buffer layer is present → V_{RB} only 10-20 V

Asymmetric IGBT (punchthrough IGBT)

- If buffer layer is **not** present → $V_{RB} = V_{BD}$

Symmetric IGBT (non punchthrough IGBT9

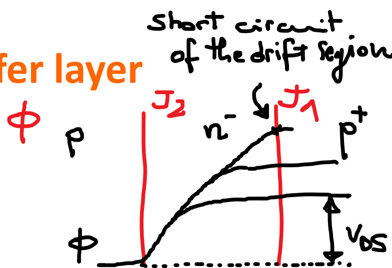
Buffer layer

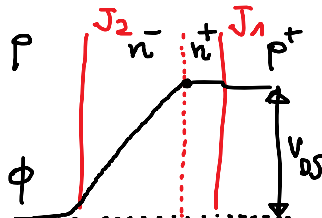
No buffer layer

- Drift region cannot be completely depleted (punchthrough implies reachthrough)

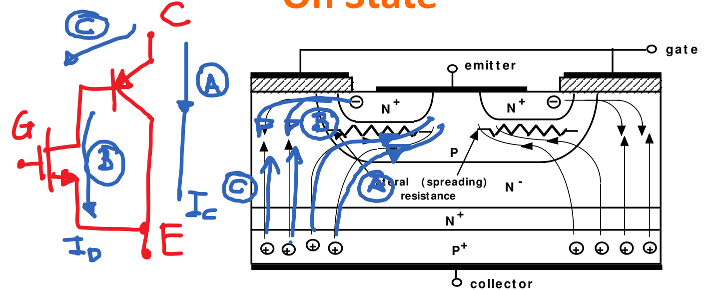
Buffer layer

- The buffer layer can totally screen the electric field and allows punchthrough.
- (same V_{BD}, lower V_{ON}, but low V_{RB})



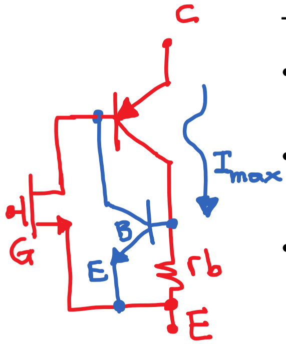


On State



- Typically $I_D > I_C$
- Lower V_{ON} than the MOSFET because "C" component causes conductivity modulation in the drift region.
- $V_{ON} = V_{J1} + R_{ON}I = 1 \div 2\text{ V} < V_{ON}$ of a MOSFET

Latch up



The npn BJT must be in cut off

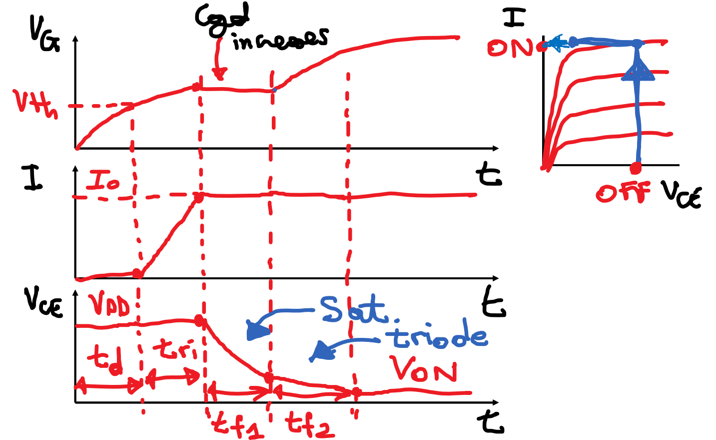
- V_{BE} depends on voltage drop on r_b.
- **Static Latch up**

  I_{MAX_Static}
- **Dynamic Latch up (during IGBT turn off*)**

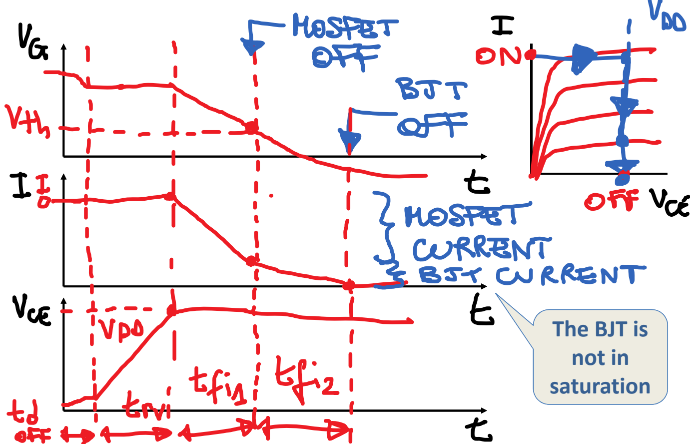
  $I_{MAX_Dynamic} < I_{MAX_Static}/2$

* During turn off the MOSFET turns off first → all IGBT current + CB displacement current can pass through rb

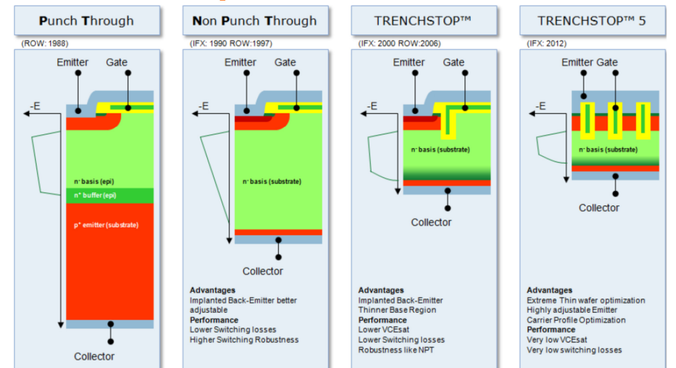
Turn on transient



Turn off transient

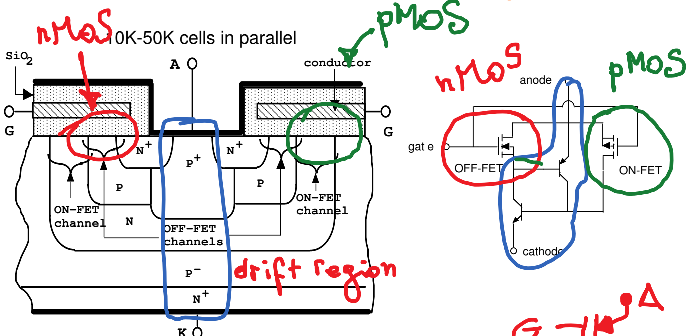


Example: Infineon IGBTs



Trenchstop 5: I_{max} 80 A, V_{BD} 650 V, V_{ON} 1.6-2 V,

MCT MOS-controlled thyristor

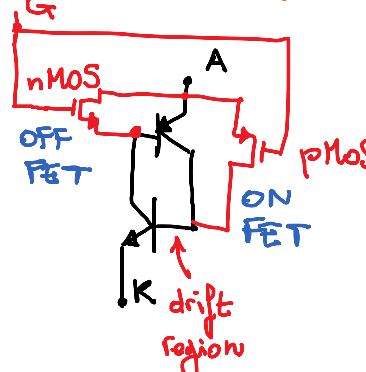


P-MCT – Drift Region p-

Harris Semiconductor

MOSFETs close to the Anode

P MCT (drift region p-)



Asymmetric Blocking (negative V_{AK})

Turn ON

The pMOS must be turned ON to feed the npn base

$$V_G < V_{TP} + V_A$$

Turn OFF

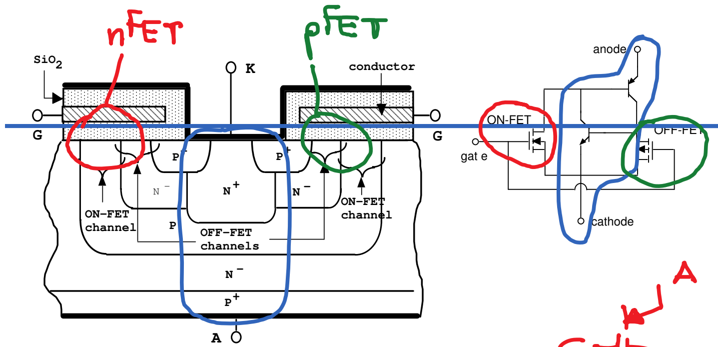
The nMOS must be turned ON to bypass the BE junction of the pnp

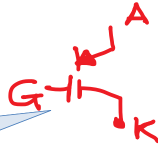
$$V_G > V_{TN} + V_{CESAT}$$

Only approx 1 in 20 cells has the ON FET

One of the two FETs is always kept ON to keep the state

N MCT (drift region n-)

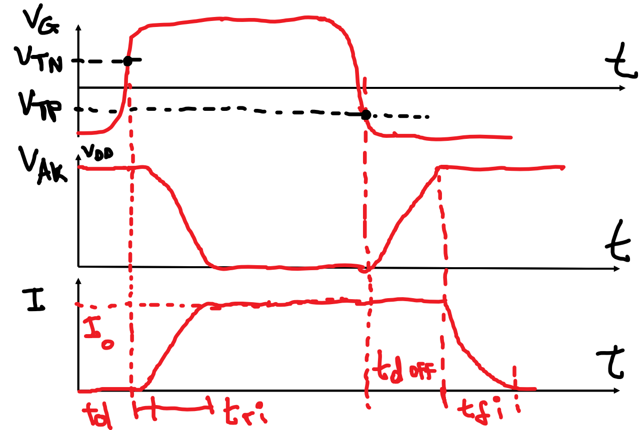




Asymmetric Blocking:
$V_{AK} > 0$

MOSFETs close to the Cathode

NMCT turn ON and OFF

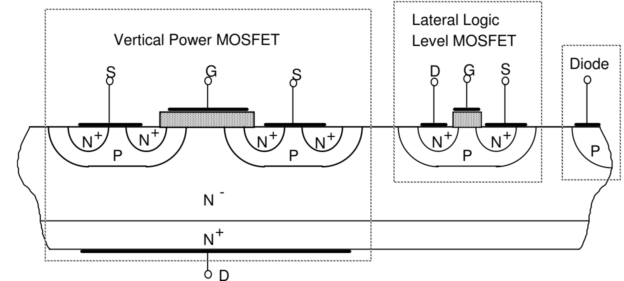


Power Integrated Circuits

1. Smart Power / Smart Switches (I < 50-100 A, V < 1KV):
2. High-Voltage Integrated Circuits (I < 50-100 A, V < 1KV)
3. Discrete Modules (Higher I V range)

Smart Power / Smart Switches (I < 50-100 A, V < 1KV):

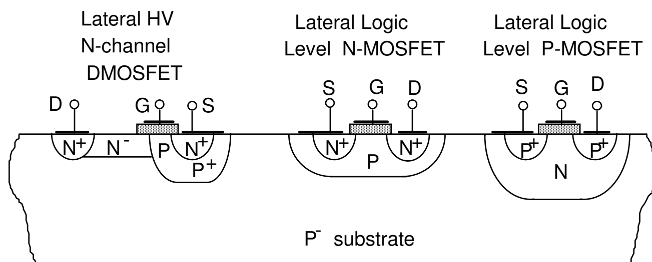
Vertical Power devices + Lateral Devices for (some) logic



If Drain of Power MOSFET at positive voltage → devices are insulated by the reversed biased p-body - n-drift region junction

High-Voltage Integrated Circuits (I < 50-100 A, V < 1KV)

High-Voltage Lateral devices + Logic devices (more complex Logic)



Self isolation

Challenges for Power Ics

- Technical
  - **Electrical isolation** of High-voltage components from Low-voltage components
  - **Thermal management** (temperature is not uniform: power devices operate at higher T than logic devices)
  - **On-chip interconnections**: high voltage conductors can disturb low voltage conductors/devices
  - Fabrication process must provide several types of devices and components
- Economical
  - **Expensive fabrication process** (large development cost) requires large volume