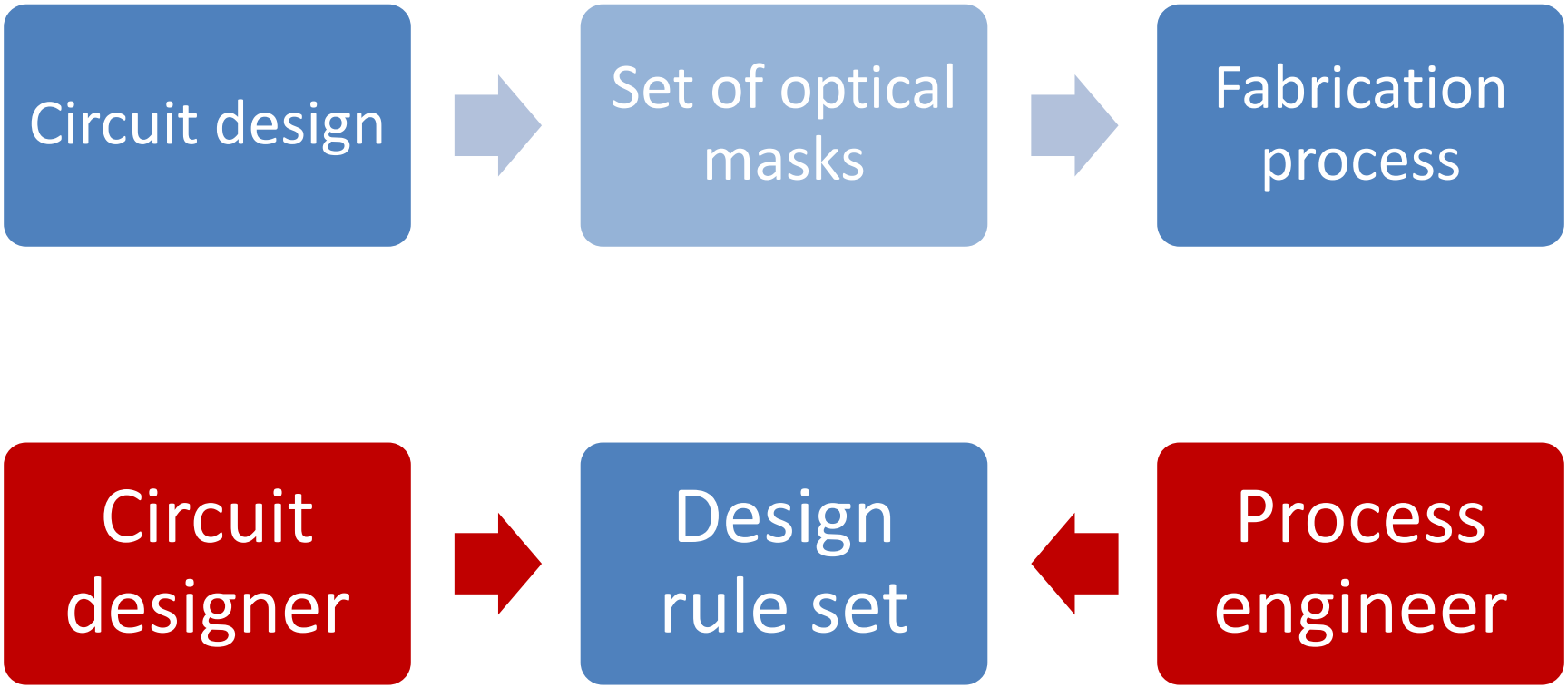
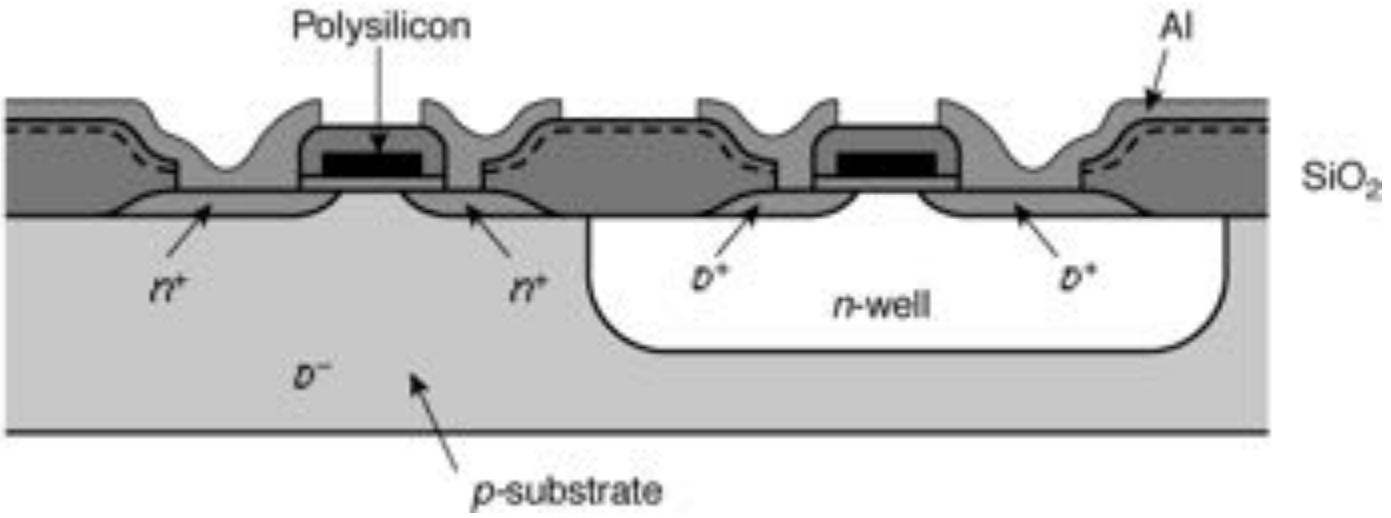
CMOS Manufacturing process



All material: Chap. 2 of J. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits, second edition, Prentice Halls, 2002

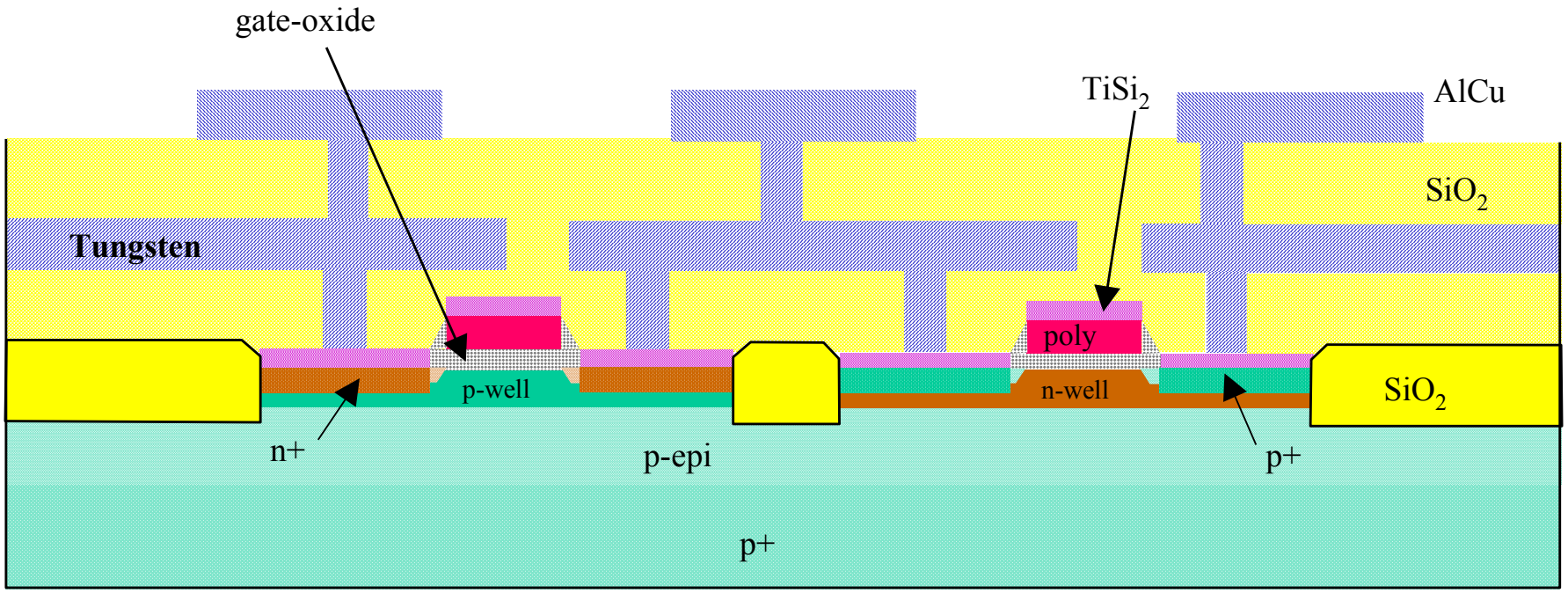
Simplified very basic CMOS Process

CMOS inverter – n-well process

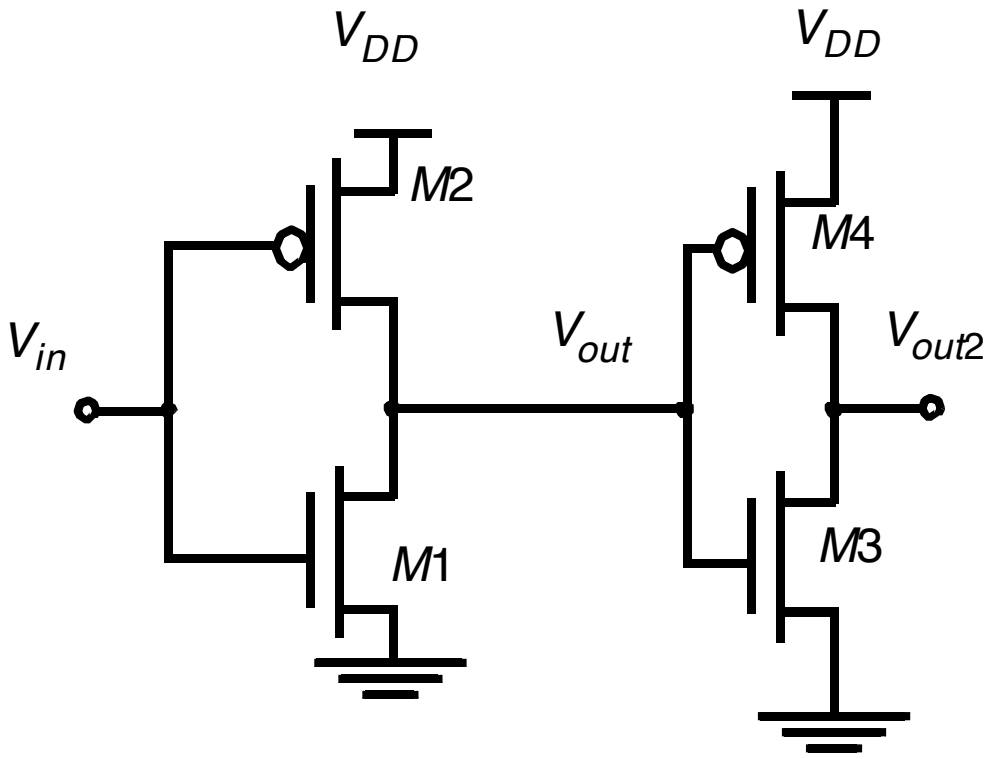


A Modern CMOS Process

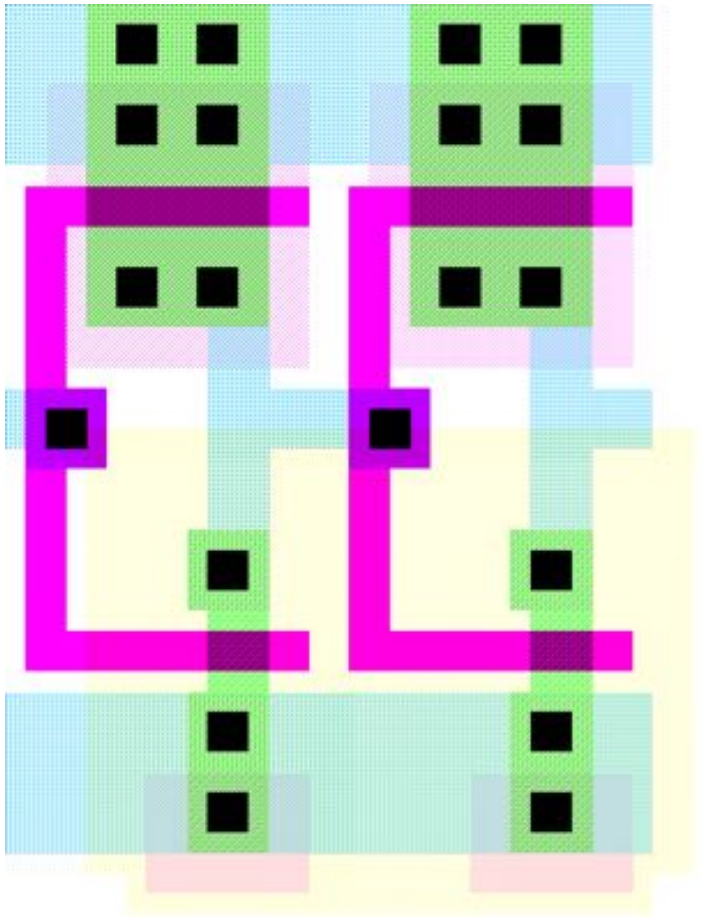
CMOS inverter – dual-well trench-isolated process



Circuit Under Design



Its Layout View



Silicon ingot

Diameter
12 inches
(300 mm)

Weight
100 Kg

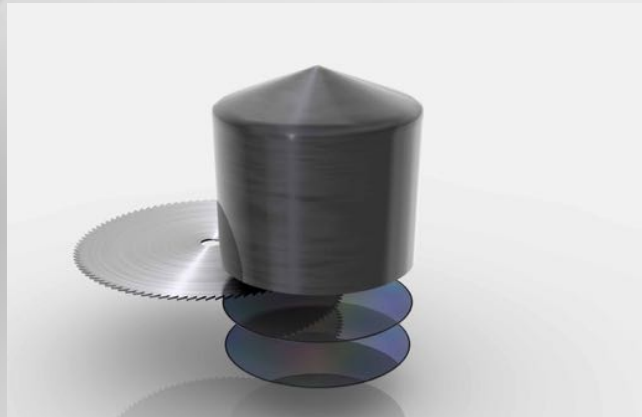
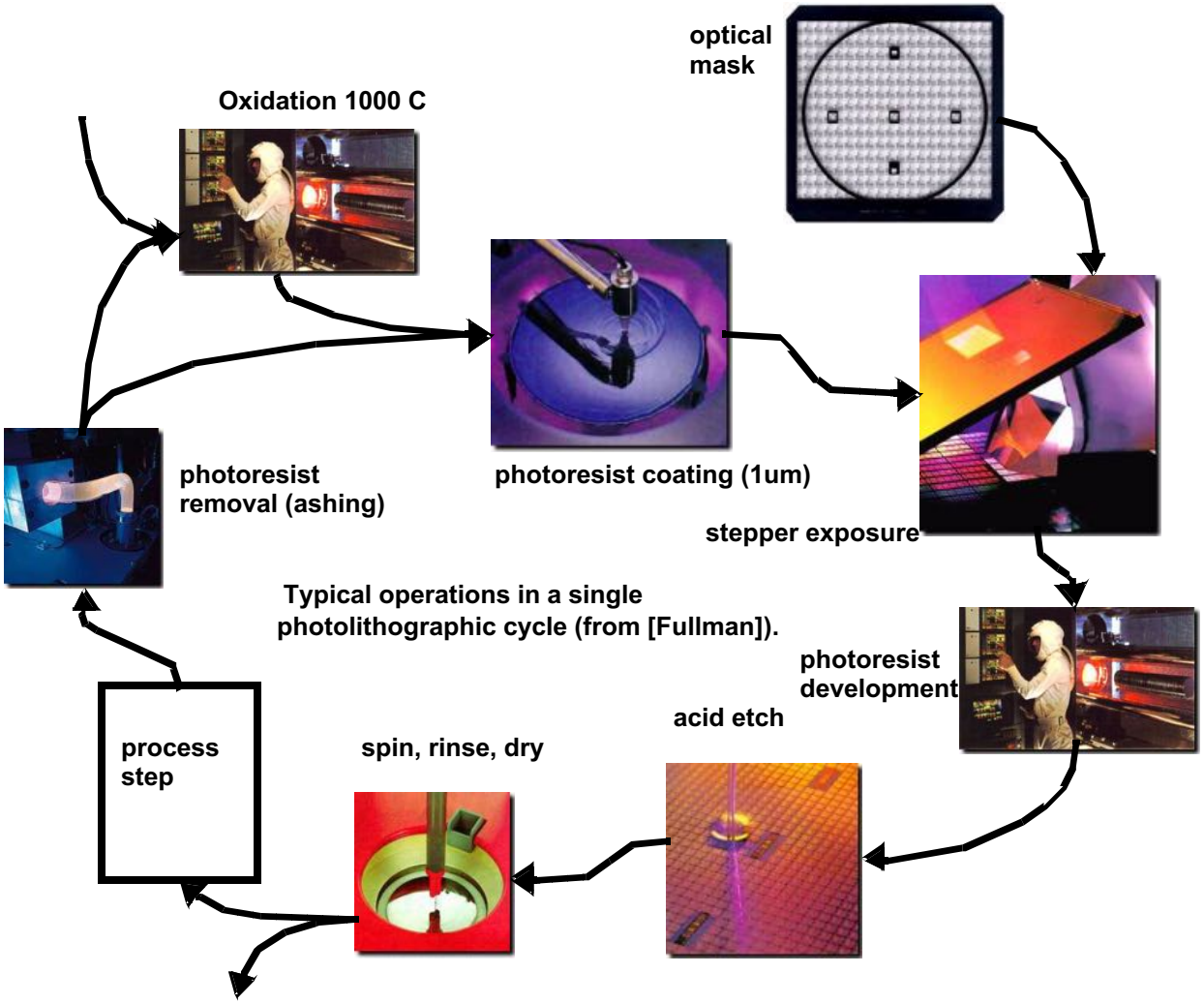


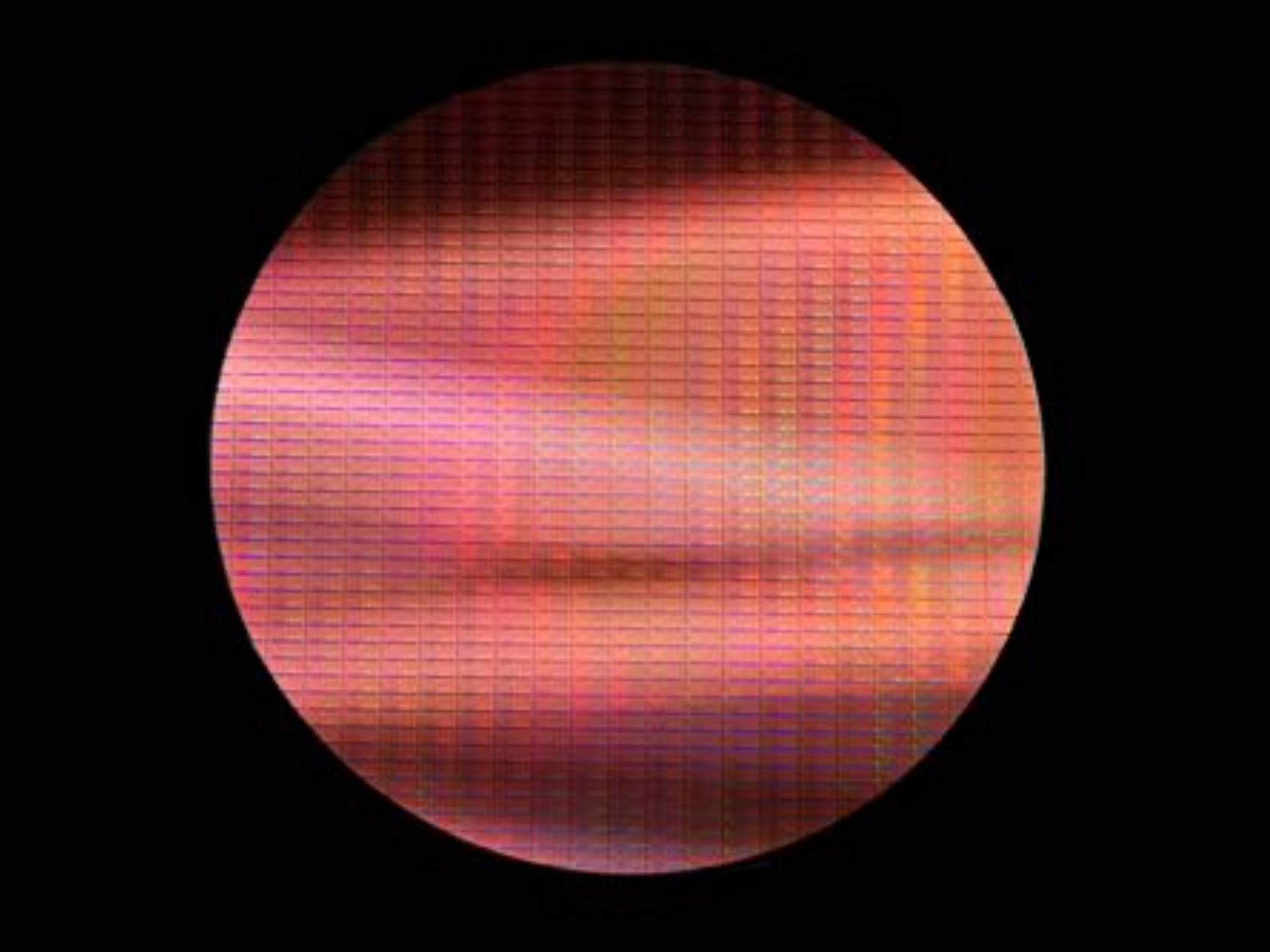
Photo-Lithographic Process

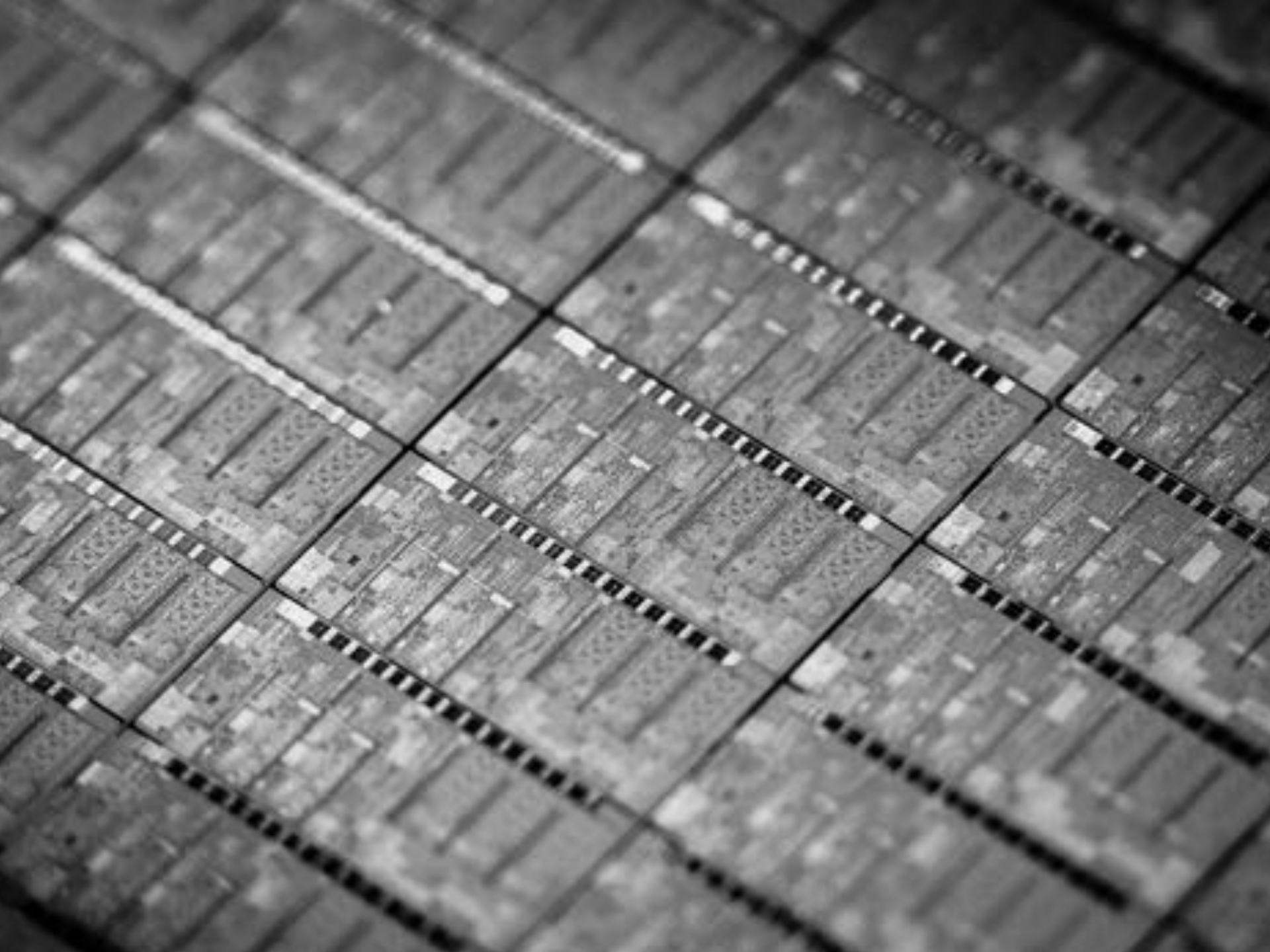


Clean room (class 1-10)

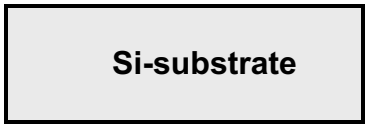
Def:
Class 1: <1 dust particle per cubic foot

In each processing step, an area of the chip is masked out using optical masks, so that the process step is selectively applied to the other regions

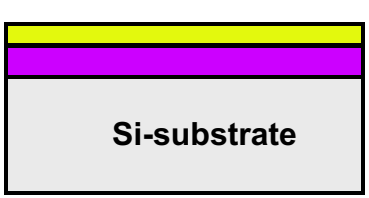




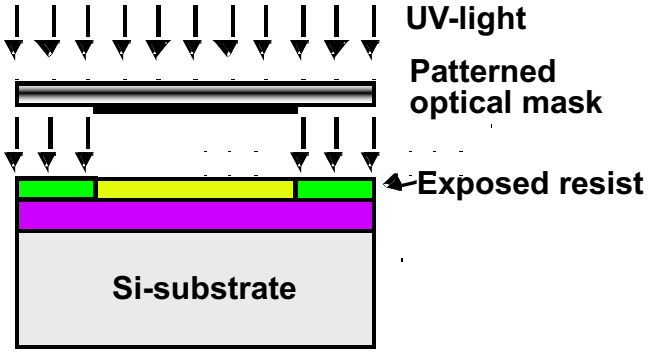
Example of process step: Patterning of SiO2



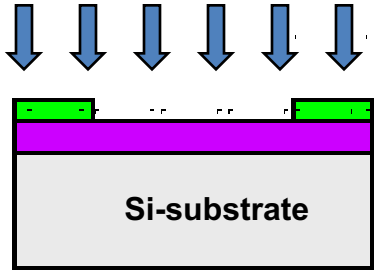
(a) Silicon base material



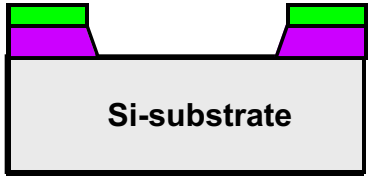
(b) After oxidation and deposition of negative photoresist



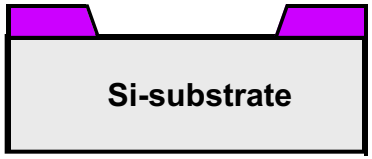
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2



(e) After etching



(f) Final result after removal of resist

Recurring process steps (1/2)

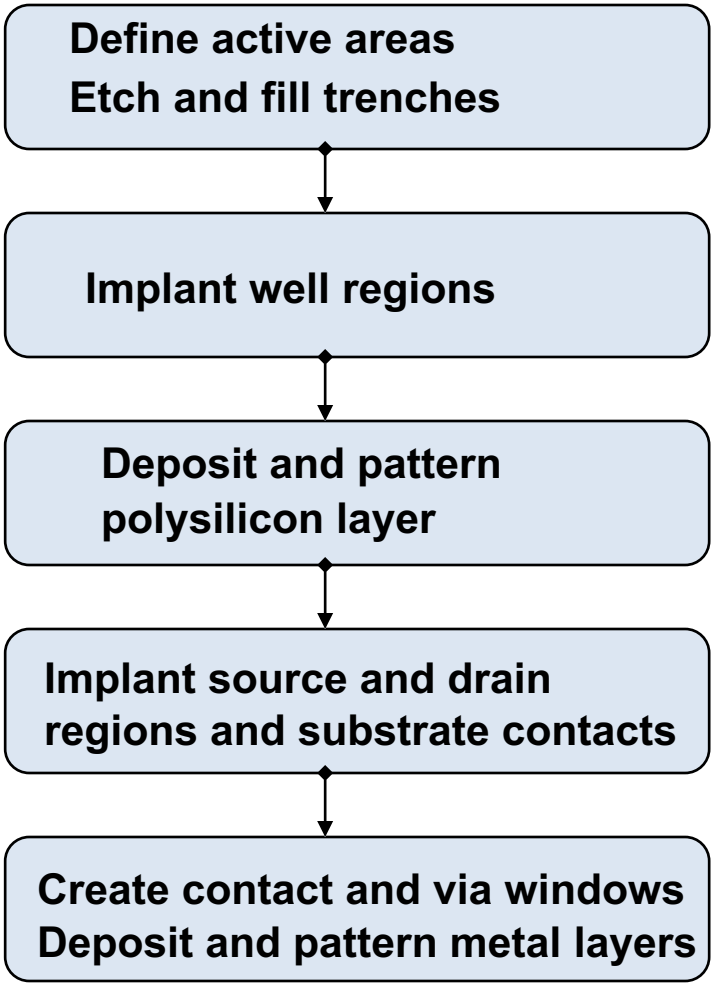
- **Doping**
  - **Diffusion** (gas with dopant, 900-1100 ^{o}C)
  - **Ion implantation**
    - Lattice damage (displacement of atoms)

    → **Annealing** step (1000 ^{o}C for 15-30' + slow cooling)
- **Deposition** (of layers over the complete wafer)
  - **Oxidation** [silicon oxide]
  - **Chemical Vapor Deposition**: gas phase + heat (850 ^{o}C) [silicon nitride]
  - **Chemical deposition** (polysilicon: silane (SiH_4) gas over heated wafer (600 ^{o}C) → reaction an polysilicon formation
  - **Sputtering** (for aluminum): evaporation in vacuum chamber

Recurring process steps (2/2)

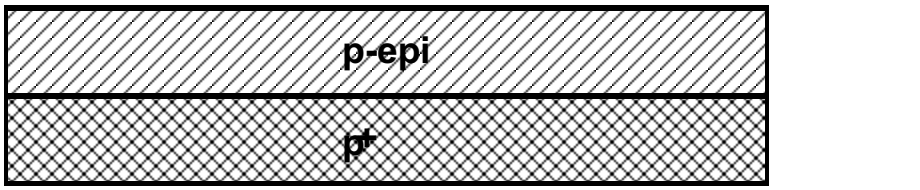
- **Etching (defines 3D patterns on the surface)**
  - **Wet etching** (with acid or basic solutions)
    - e.g. Hydrofluoric acid for silicon oxide
    - Almost isotropic
  - **Dry or plasma etching**
    - Plasma: mix of nitrogen, chlorine, boron trichloride
    - Strongly anisotropic (steep vertical edges)
- **Planarization (**flatten the surface to allow layer deposition)
  - **Chemical Mechanical Polishing (CMP)**
    - Liquid carrier with a suspended abrasive component

Simplified CMOS Process flow

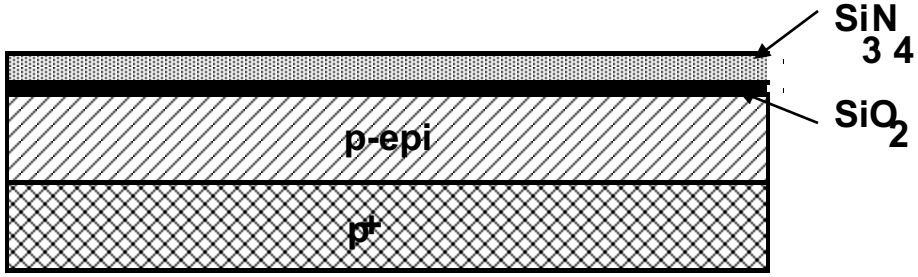


- Active areas: where transistors are
- Field oxide: insulator between neighboring devices
- Wells in the active areas
- Gate stack
- Contact doping
- Metal Interconnects

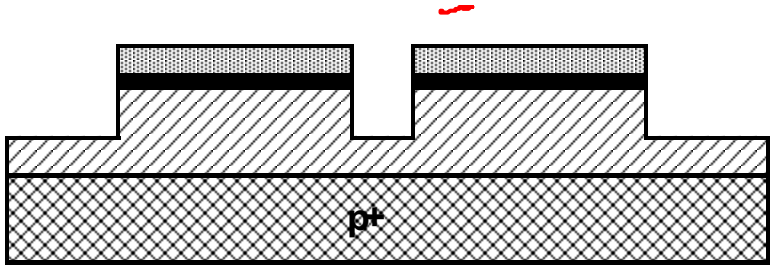
CMOS Process Walk-Through



(a) Base material: p+ substrate with p-epi layer

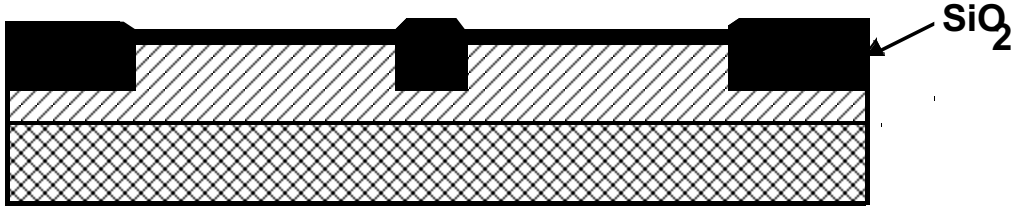


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

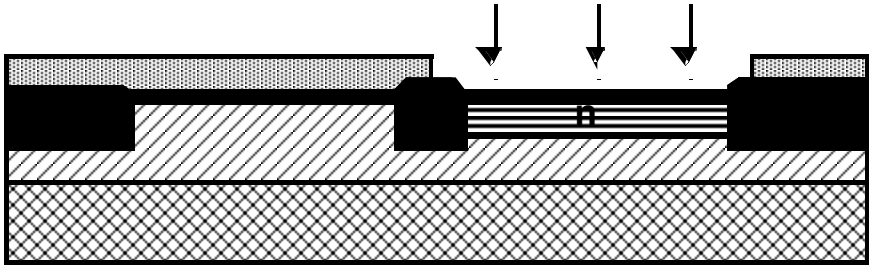


(c) After plasma etch of insulating trenches using the inverse of the active area mask

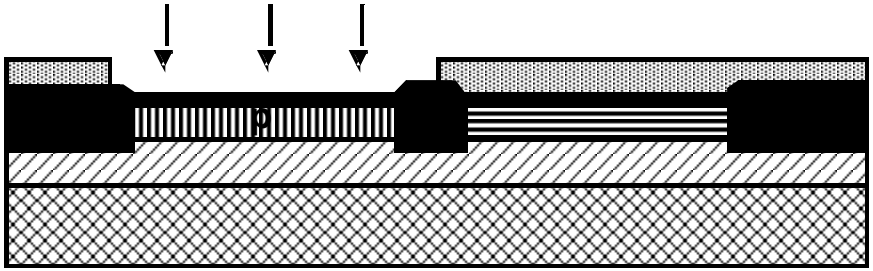
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

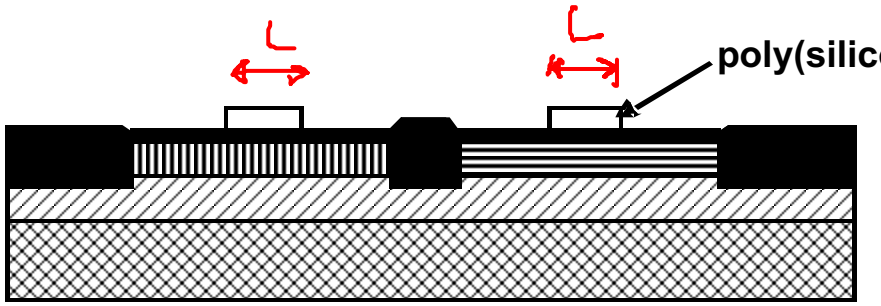


(e) After n-well and V_{Tp} adjust implants



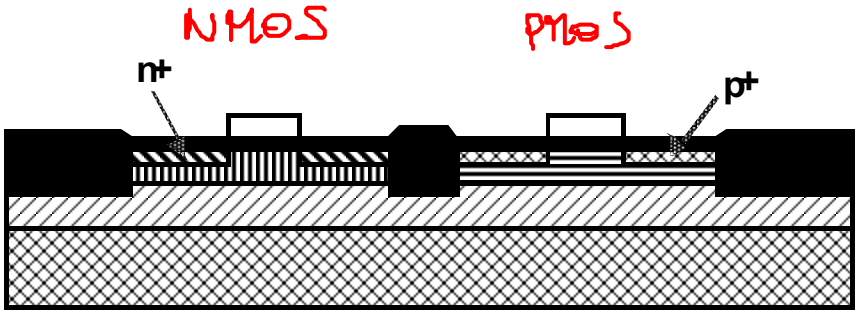
(f) After p-well and V_{Tn} adjust implants

CMOS Process Walk-Through

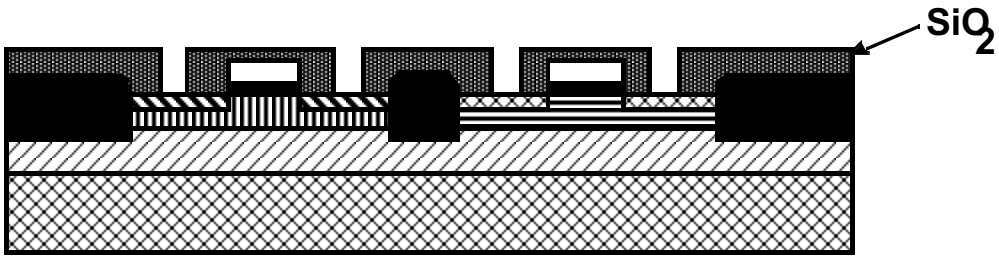


SELF-ALIGNED PROCESS

(g) After polysilicon deposition and etch

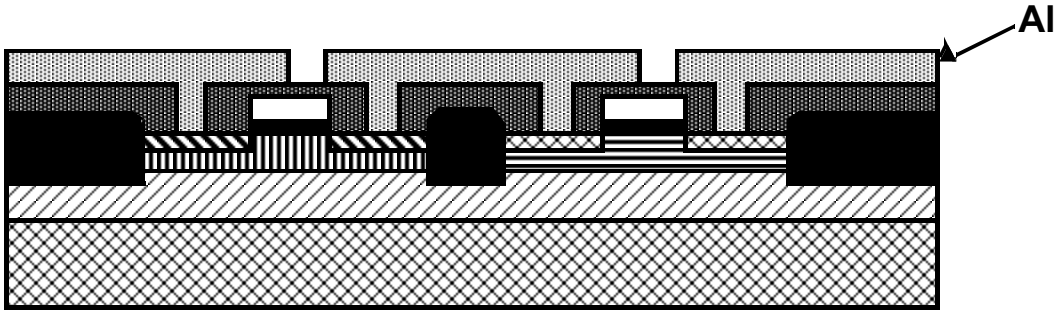


(h) After n+ source/drain and p+ source/drain implants. These steps also dope the polysilicon.

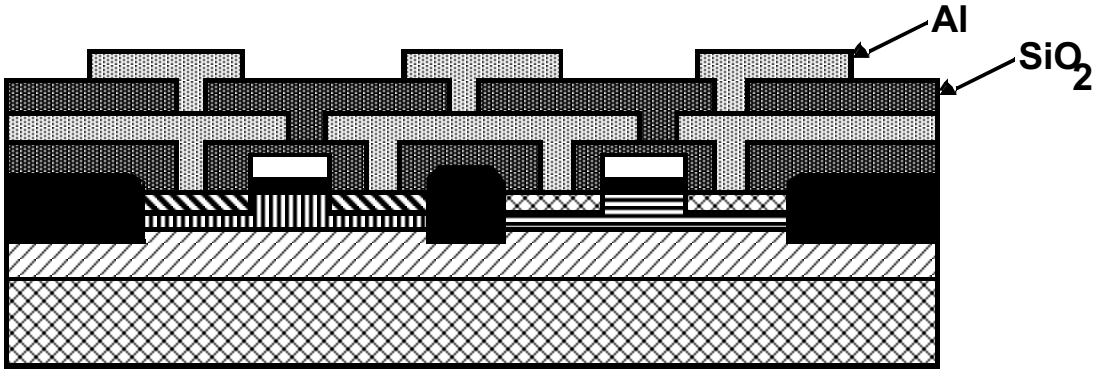


(i) After deposition of SiO_2 insulator and contact hole etch.

CMOS Process Walk-Through

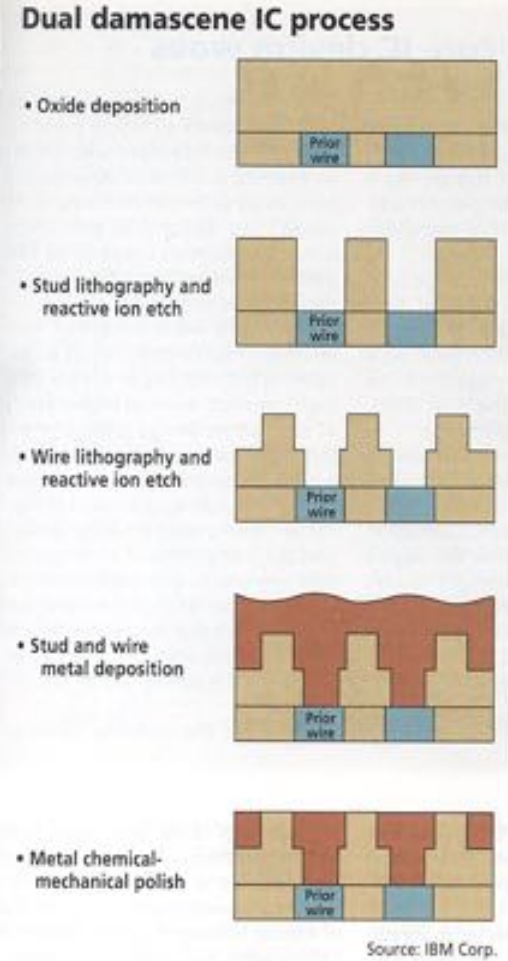


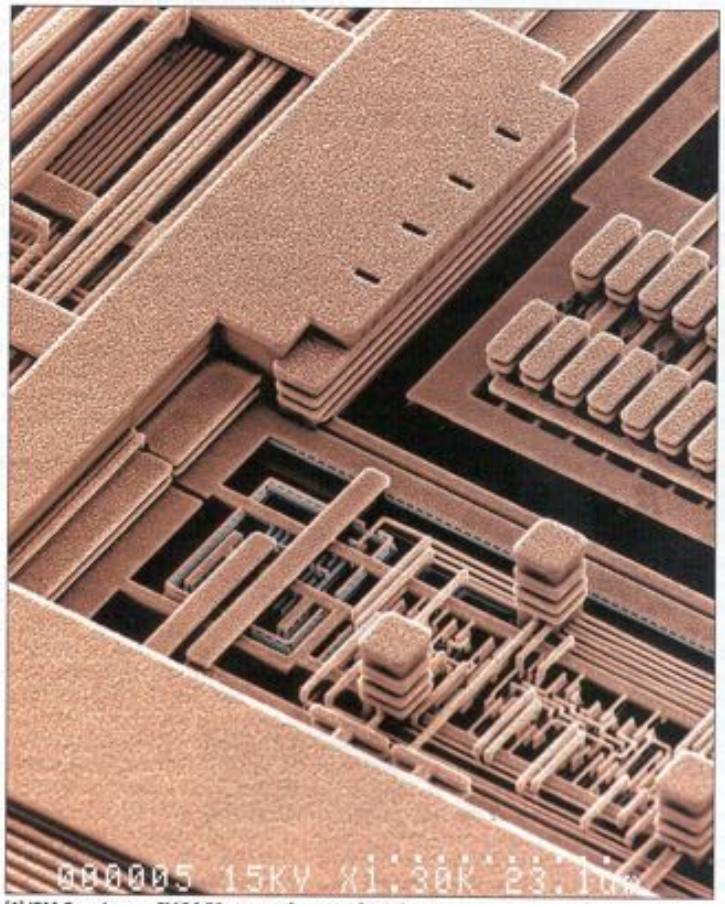
(j) After deposition and patterning of first Al layer.



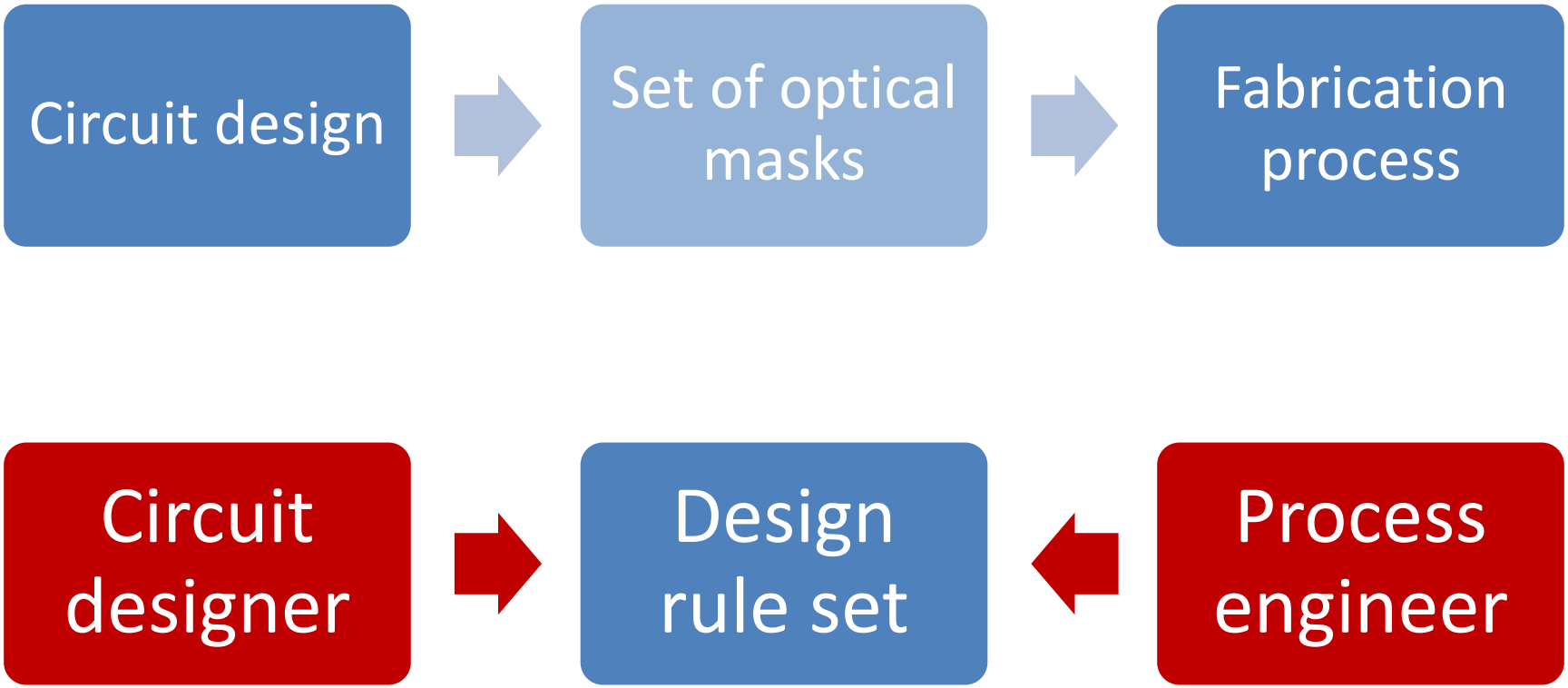
(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

Advanced Metallization





CMOS Manufacturing process

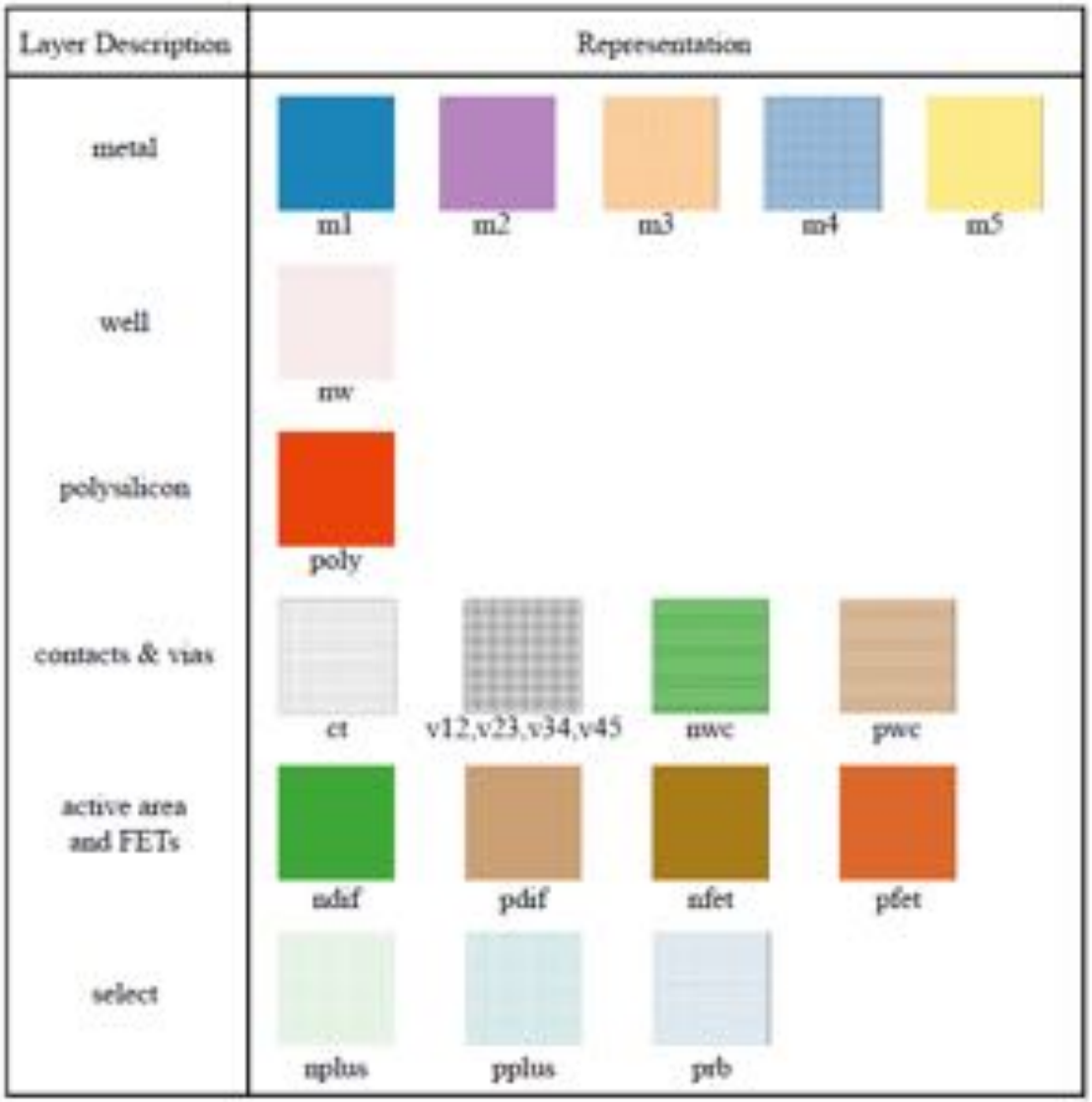


All material: Chap. 2 of J. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits, second edition, Prentice Halls, 2002

Design Rules

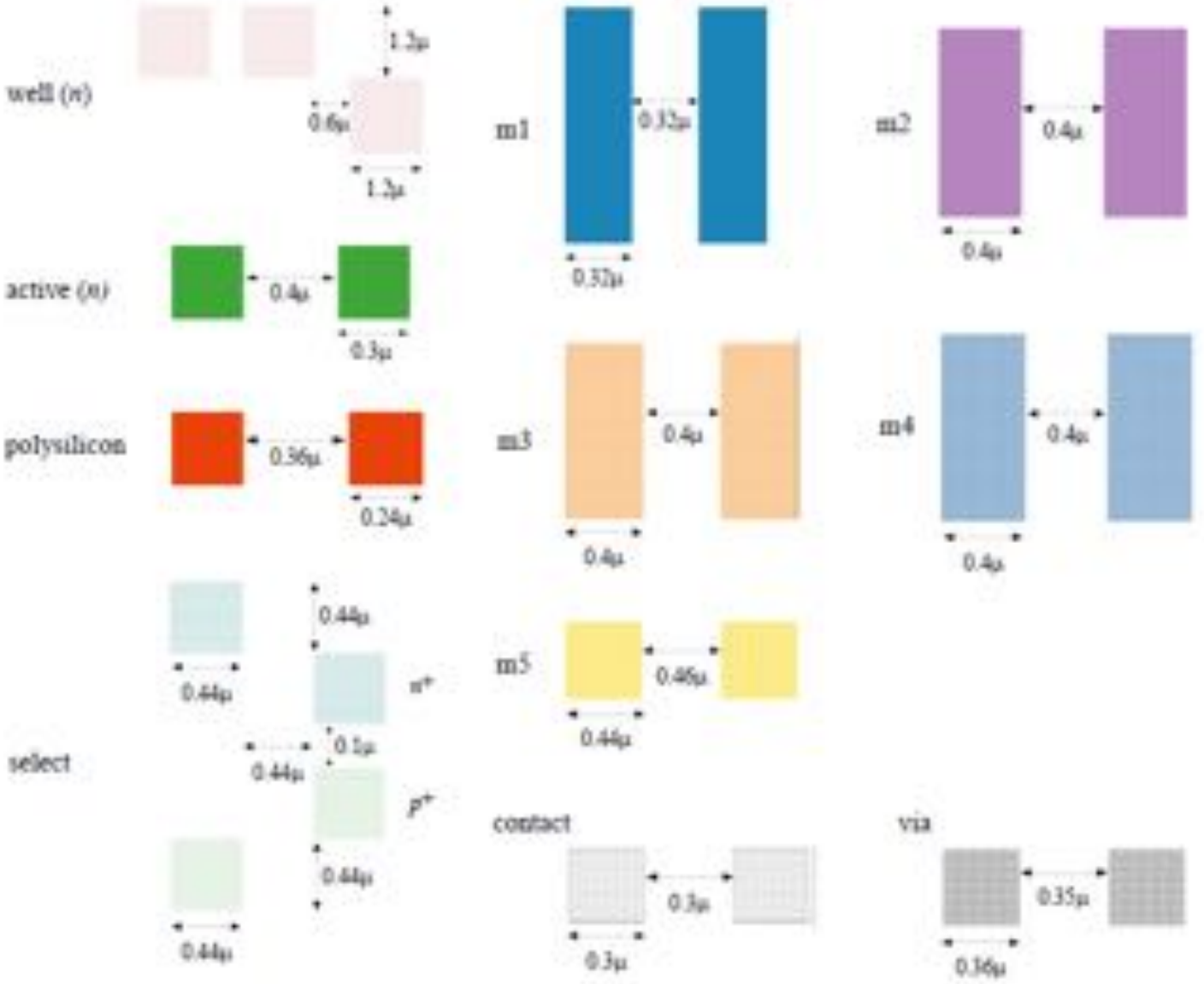
- Minimum line width depend on **lithography** and **process**
- **Micron rules: absolute dimensions** for intra-layer and inter-layer layouts

Layers in 0.25 μm CMOS process



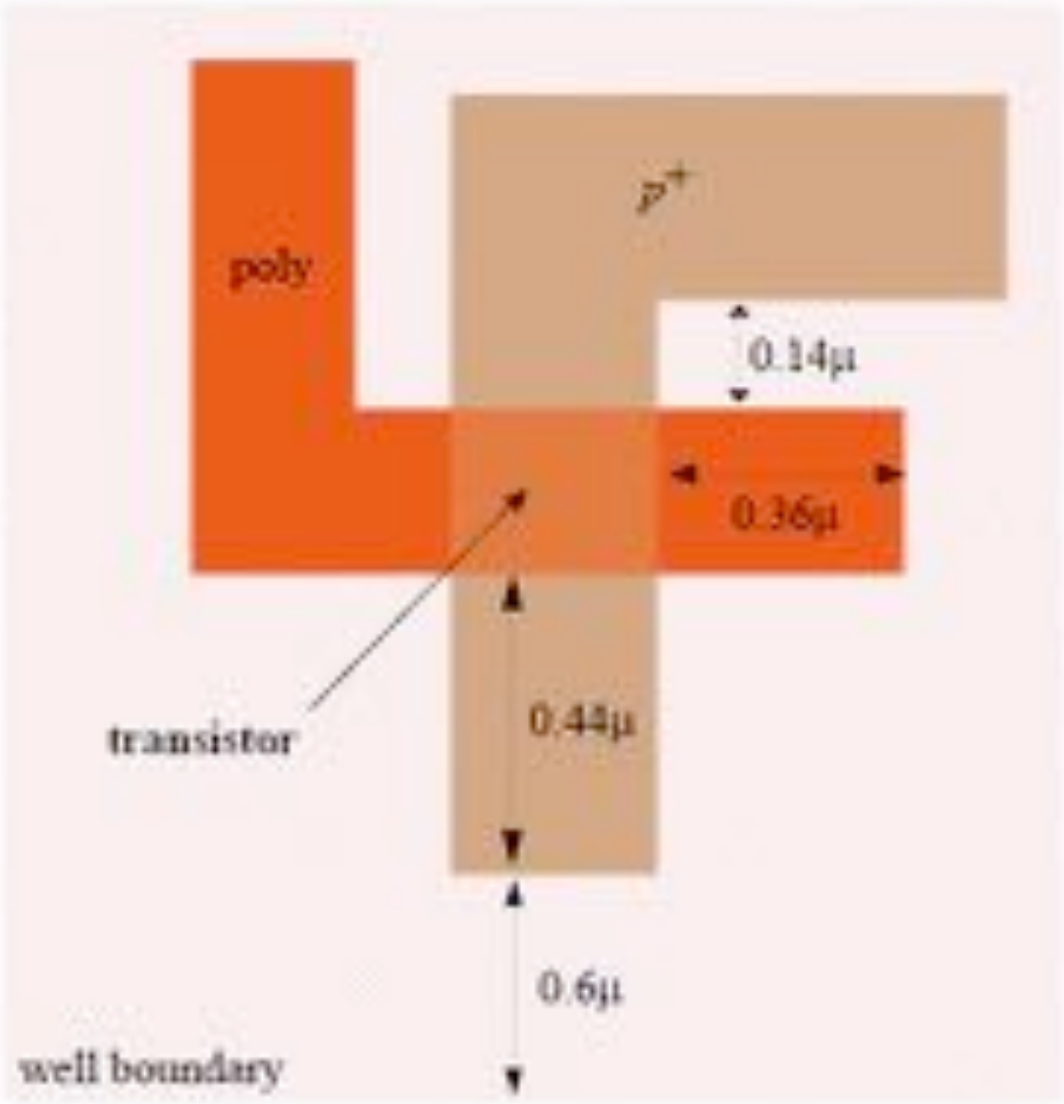
Colorplate 1. CMOS layers and representations (for vanilla 0.25 μm CMOS process)

Intra-Layer Design Rules



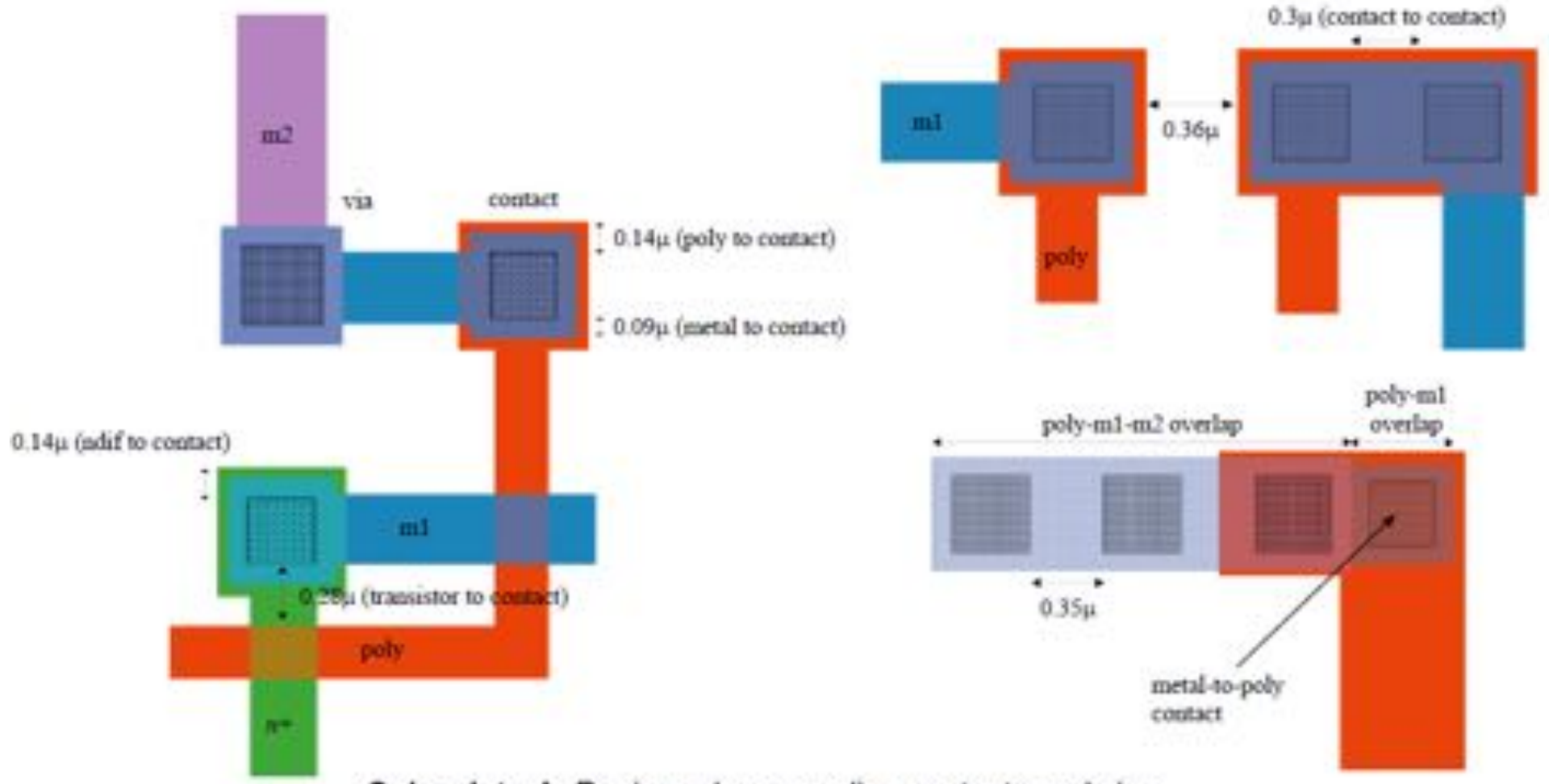
Colorplate 2. Intra-layer layout design rules, expressed as minimum dimensions and spacings.

Transistor Layout



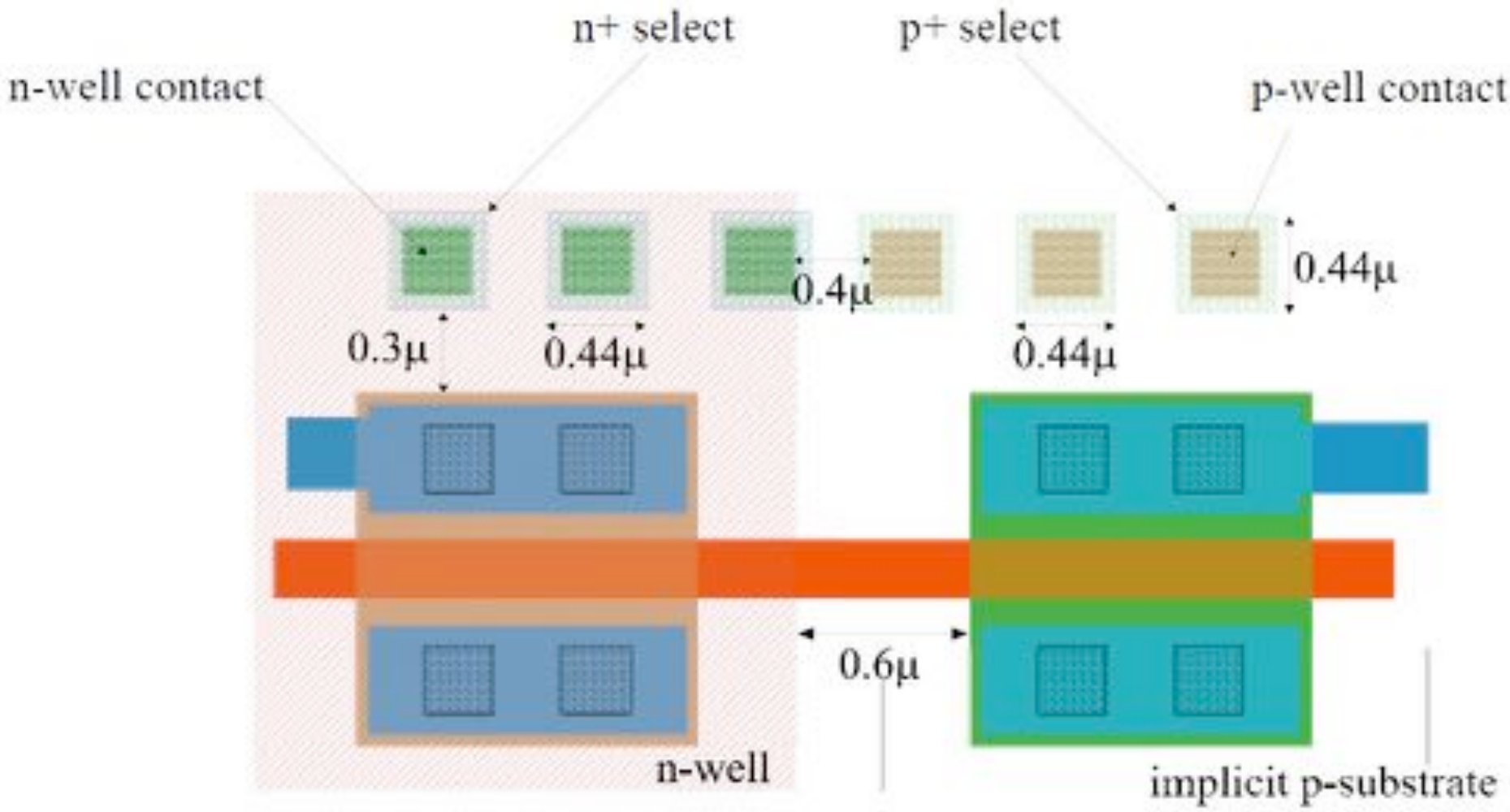
Colorplate 3. Design rules concerning transistor layout. The device shown is a PMOS transistor.

Vias and Contacts



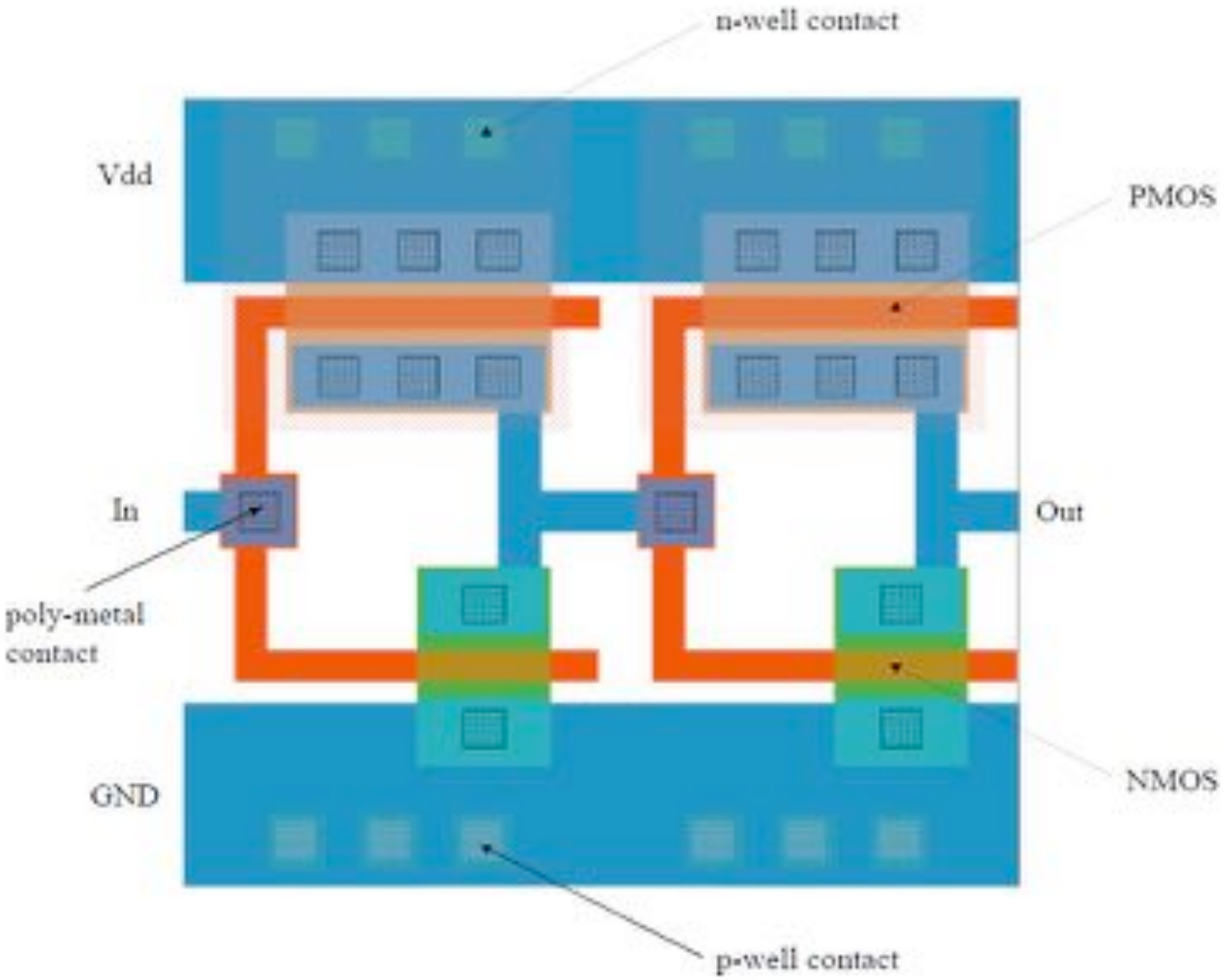
Colorplate 4. Design rules regarding contacts and vias. Overlapping layers are marked by merged colors.

Select Layer



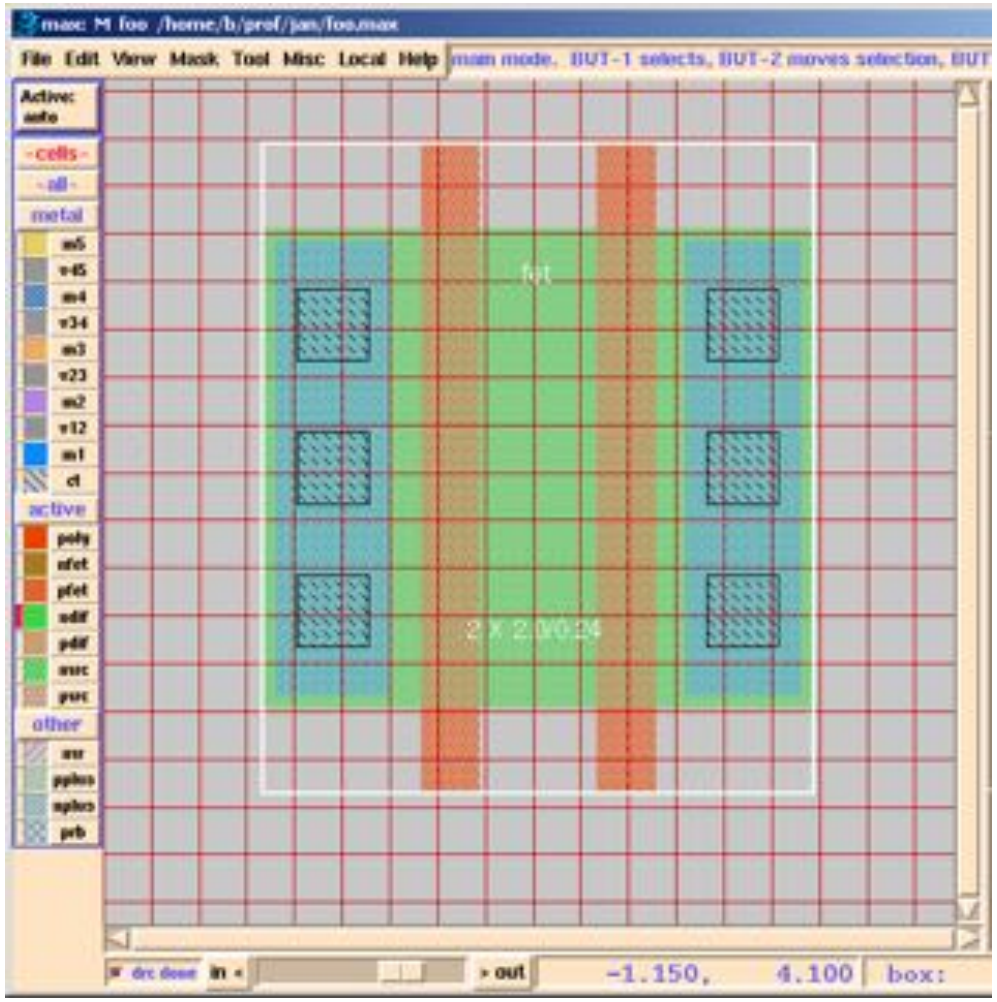
Colorplate 5. Design rules regarding well contacts and select layers.

CMOS Inverter Layout

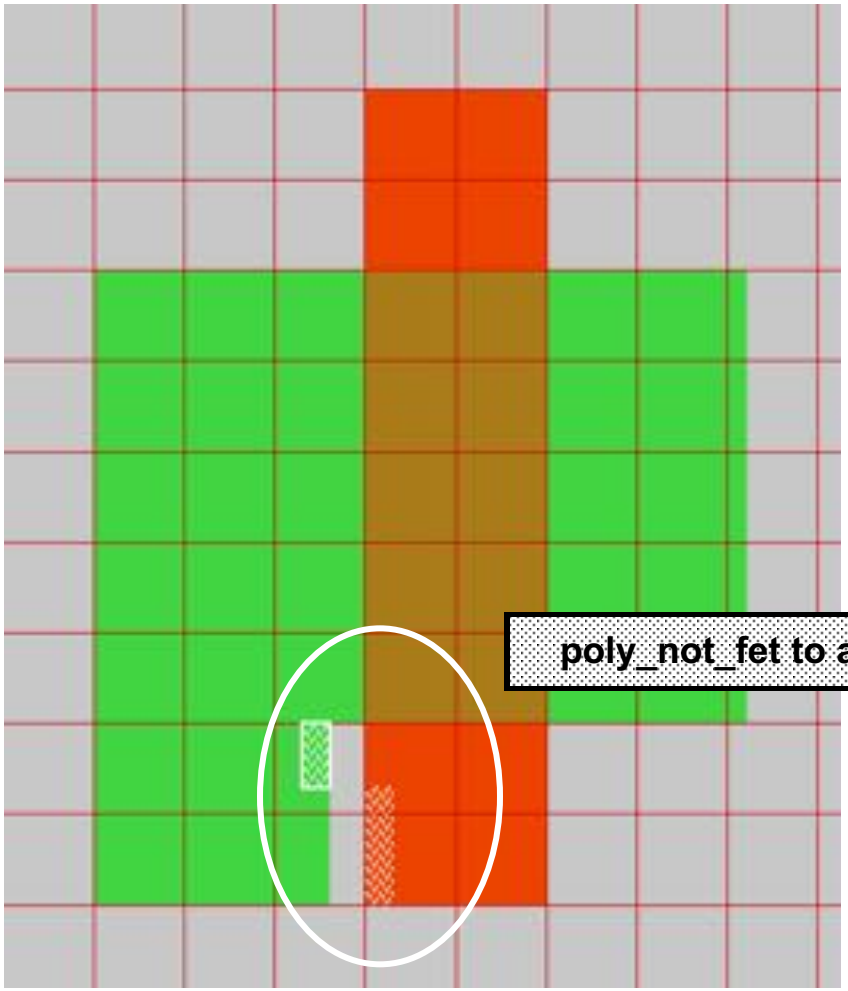


Colorplate 6. Layout of inverter in 0.25 μm CMOS technology.

Layout Editor

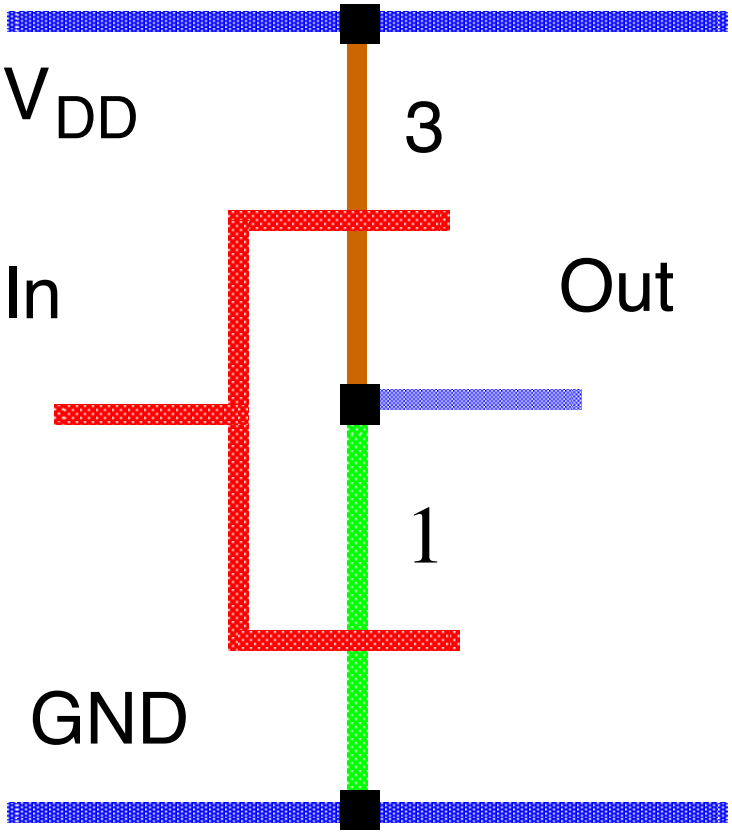


Design Rule Checker



poly_not_fet to all_diff minimum spacing = 0.14 um.

Sticks Diagram



Stick diagram of inverter

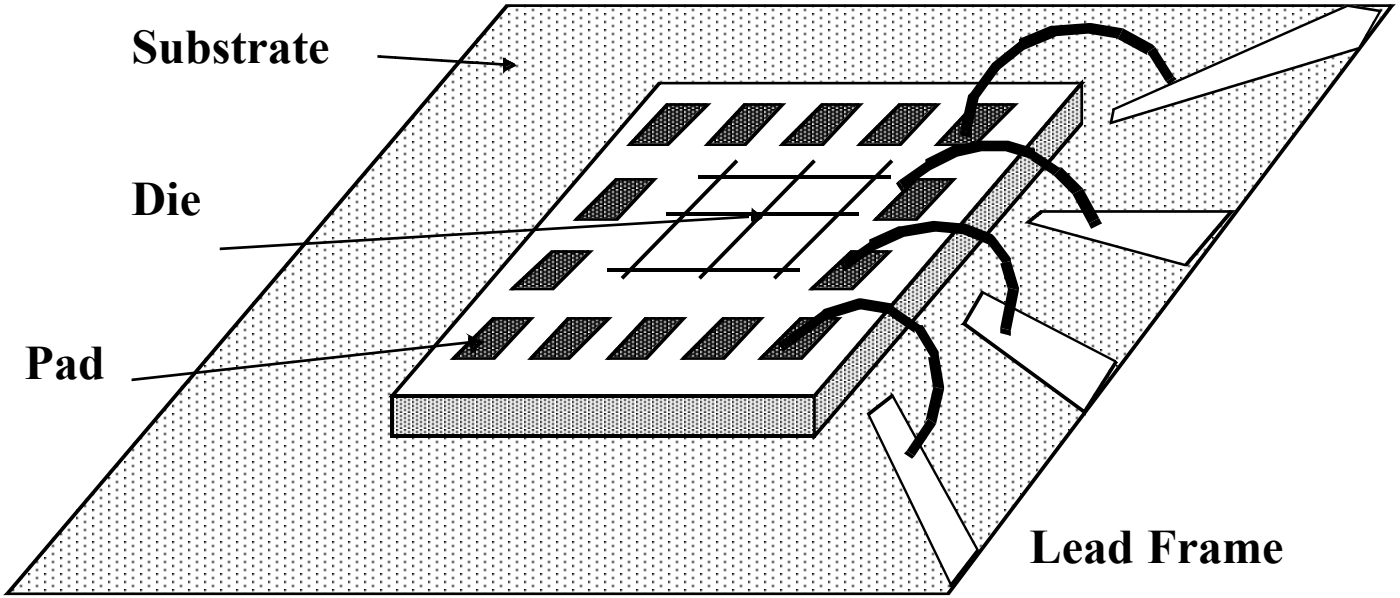
- Dimensionless layout entities
- Only topology is important
- Final layout generated by "compaction" program

Packaging Requirements

- **Electrical: Low parasitics**
- **Mechanical: Reliable and robust**
- **Thermal: Efficient heat removal**
- **Economical: Cheap**

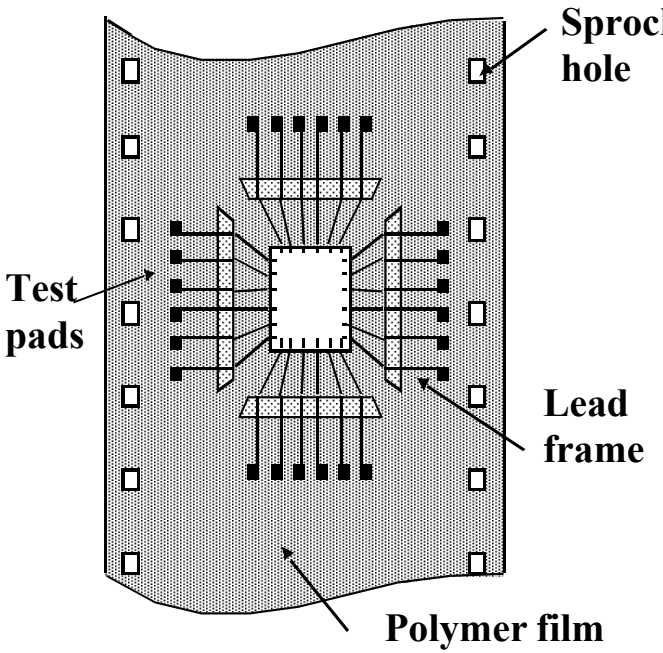
Bonding Techniques

Wire Bonding

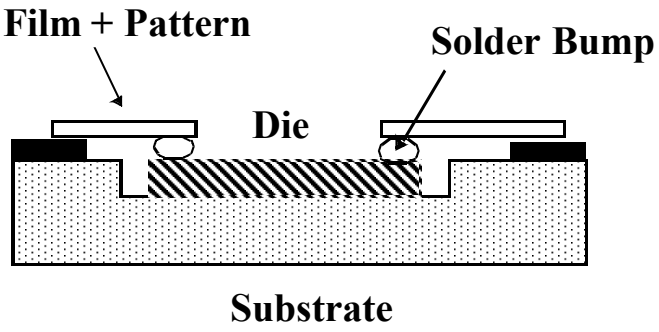


Gold wires, large inductance

Tape-Automated Bonding (TAB)

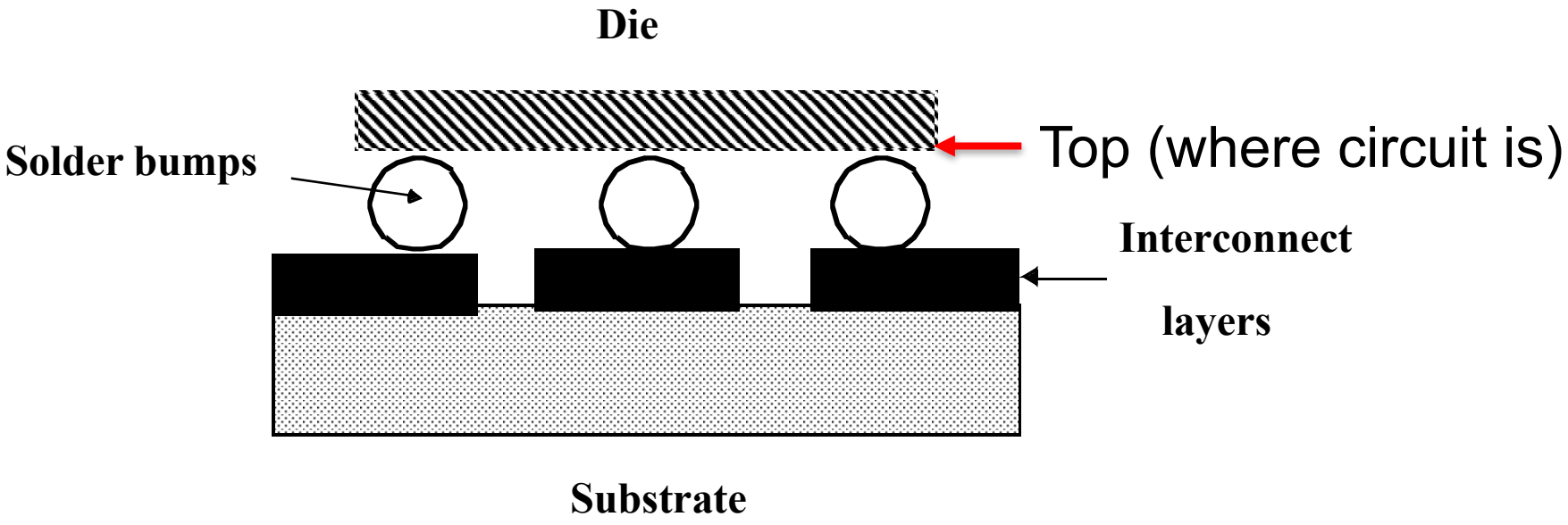


(a) Polymer Tape with imprinted wiring pattern.

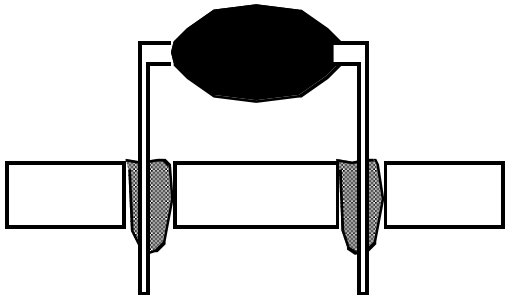


(b) Die attachment using solder bumps.

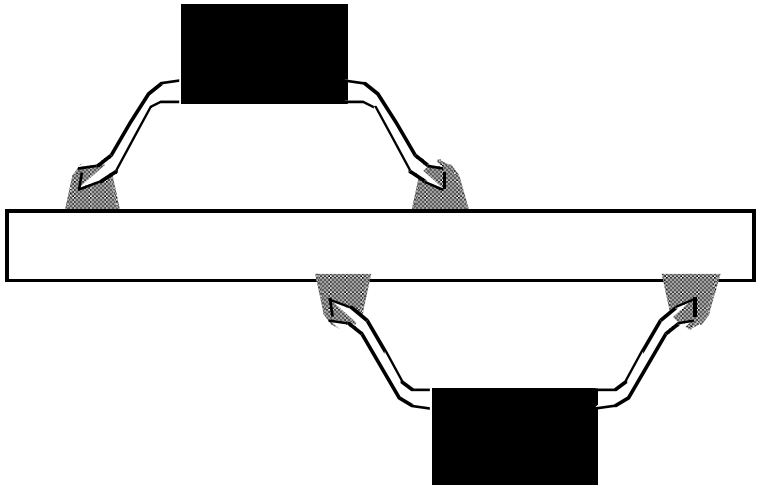
Flip-Chip Bonding



Package-to-Board Interconnect

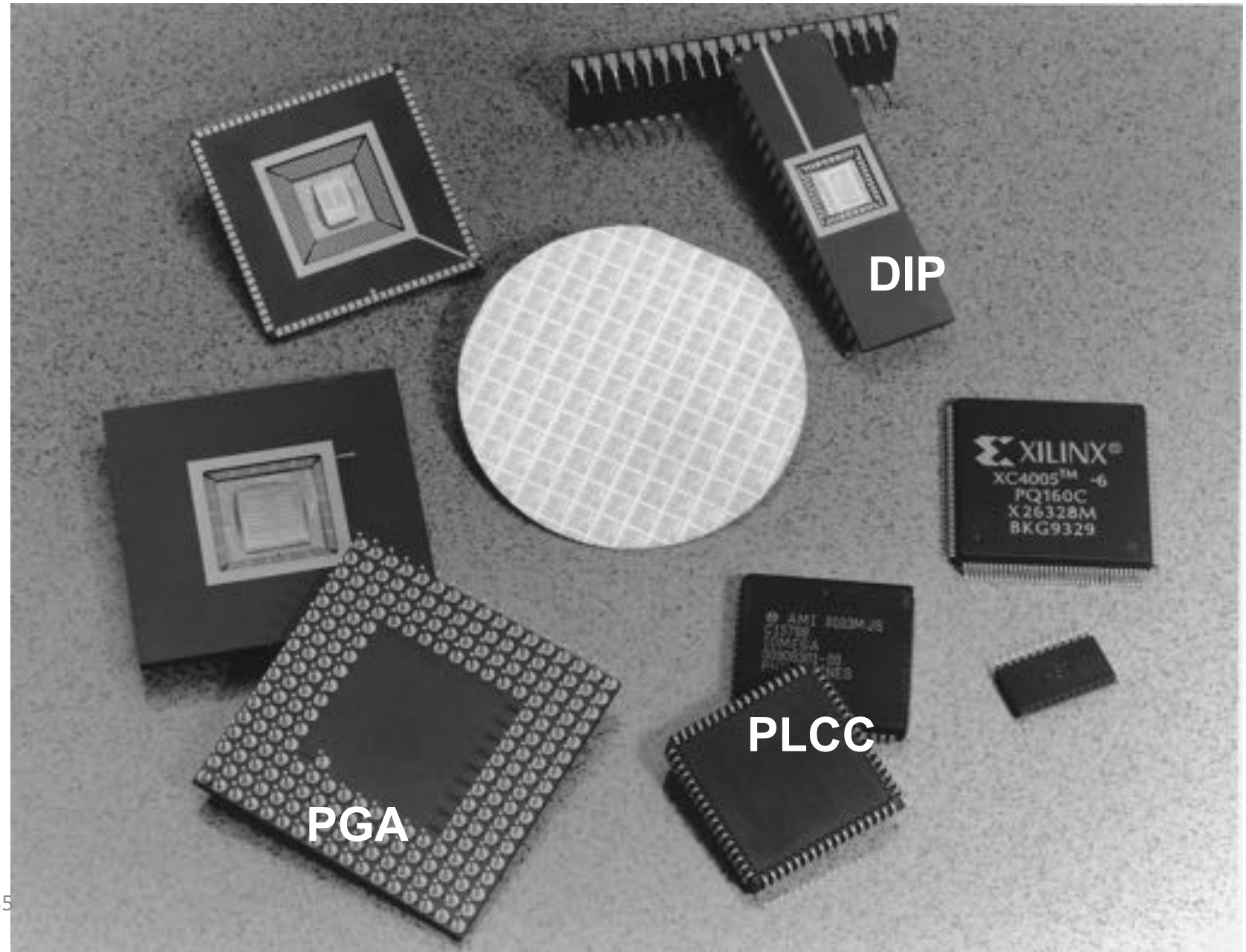


(a) Through-Hole Mounting



(b) Surface Mount

Package Types



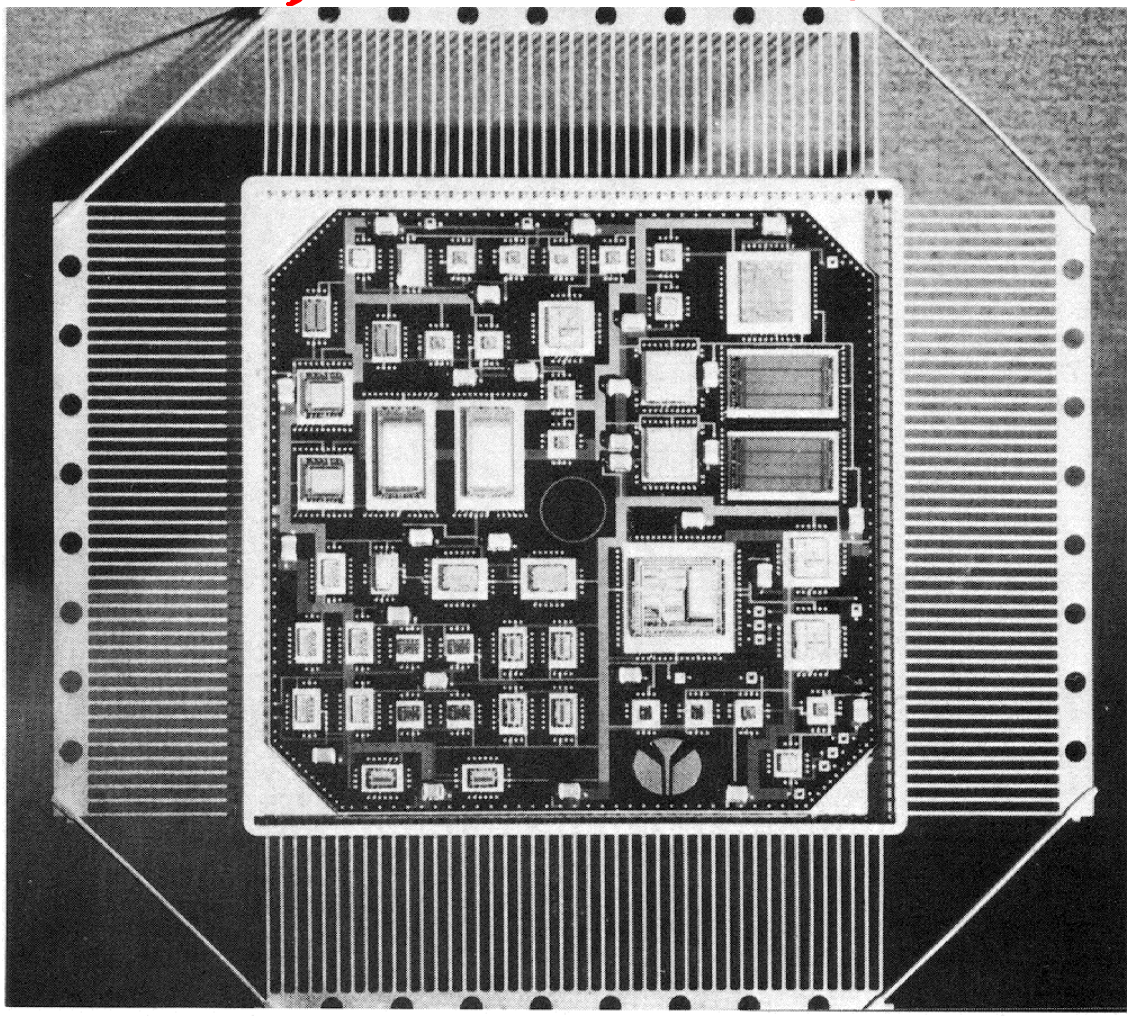
Package Parameters

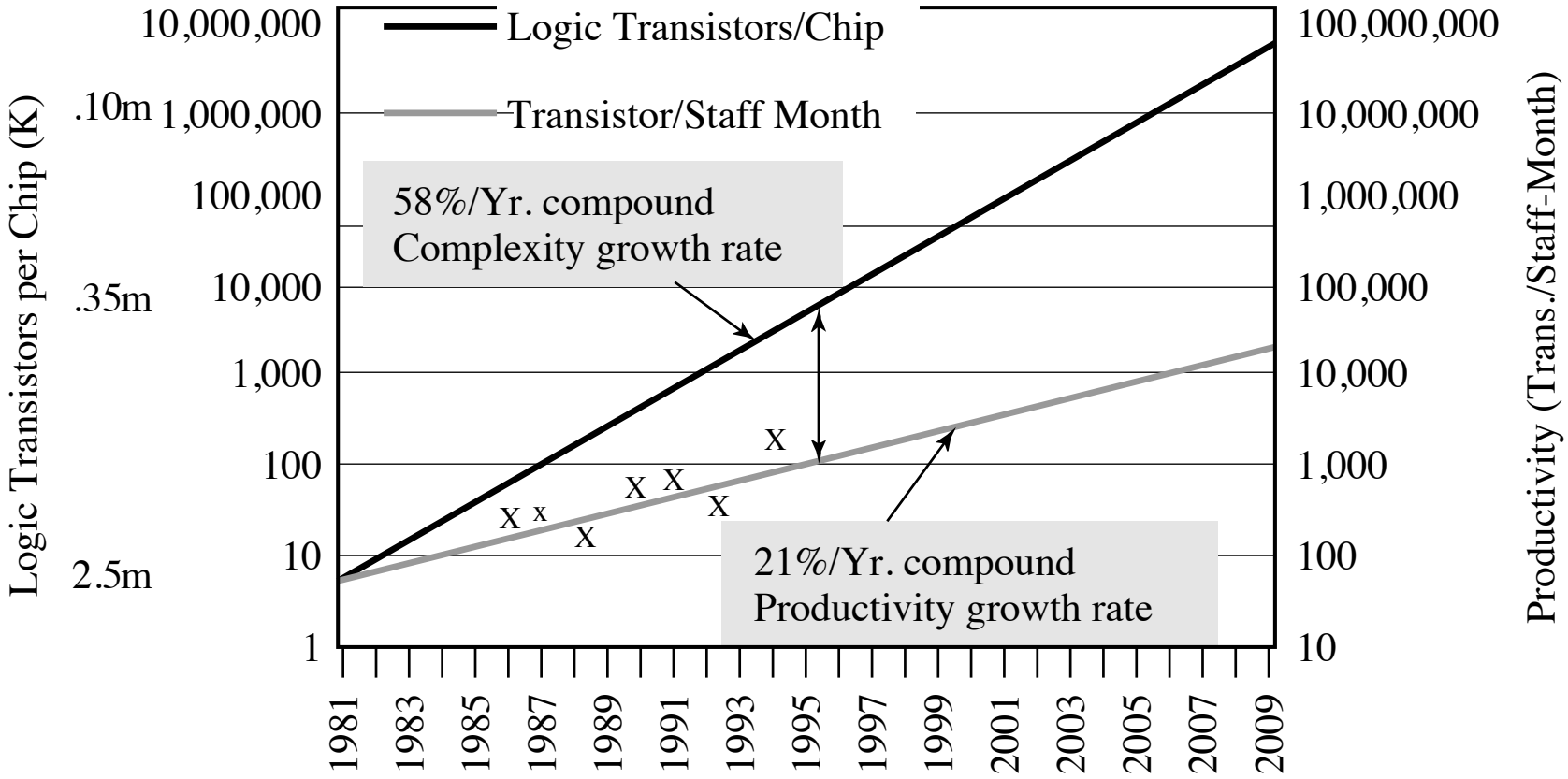
Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

Multi-Chip Modules

System on Package




Logic Transistors/Chip
Transistor/Staff Month
58%/Yr. compound
Complexity growth rate
21%/Yr. compound
Productivity growth rate
Logic Transistors per Chip (K)
Productivity (Trans./Staff-Month)
10,000,000
1,000,000
100,000
10,000
1,000
100
10
1
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000
100
10
.10m
.35m
2.5m
1981
1983
1985
1987
1989
1991
1993
1995
1997
1999
2001
2003
2005
2007
2009

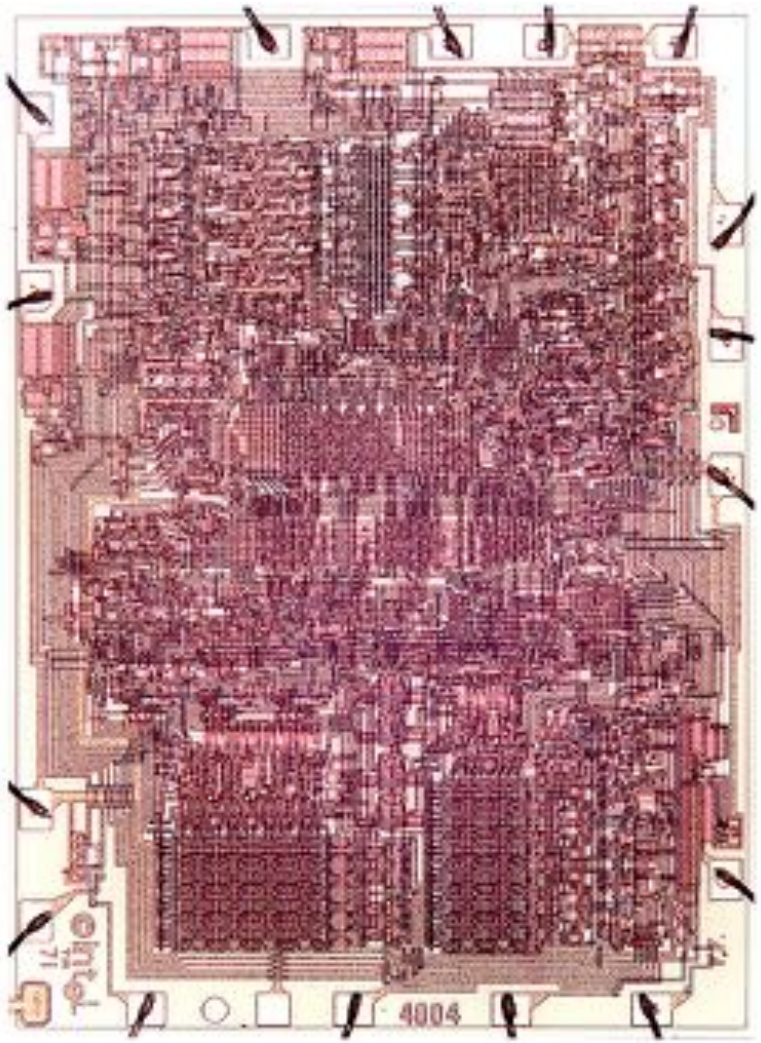
Intel 4004 – custom design

2300 PMOS

10 μm process

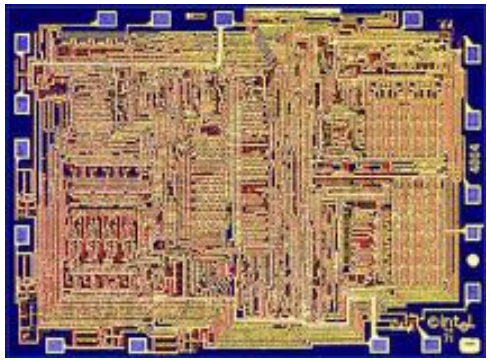
Clock:
108 KHz

Area:
3 mm x 4 mm

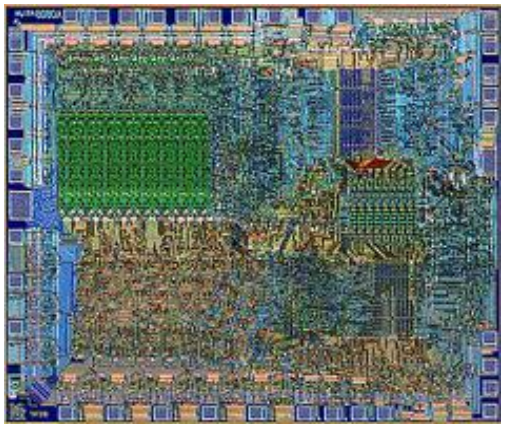


Courtesy Intel

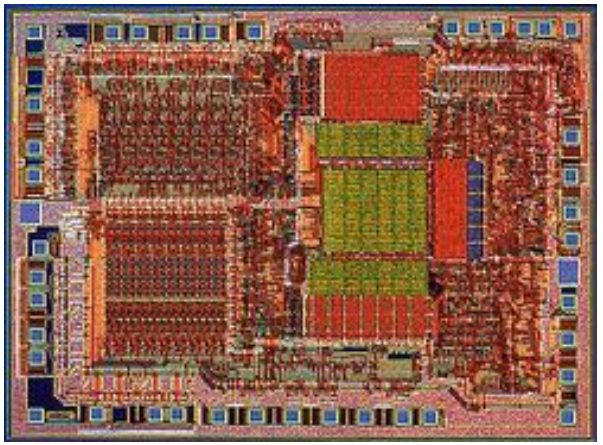
Transition to Automation and Regular Structures



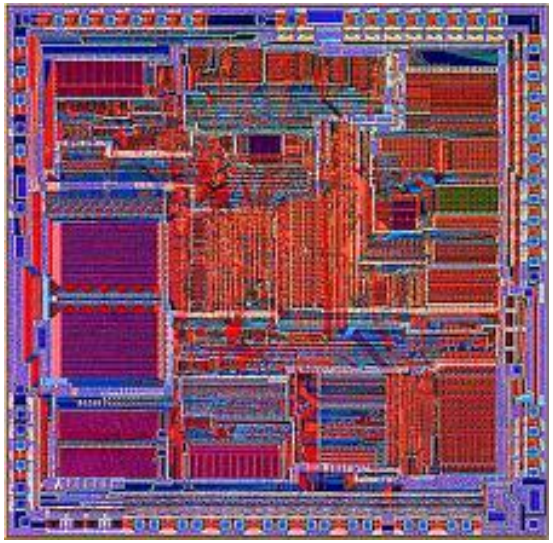
Intel 4004 (‘71)



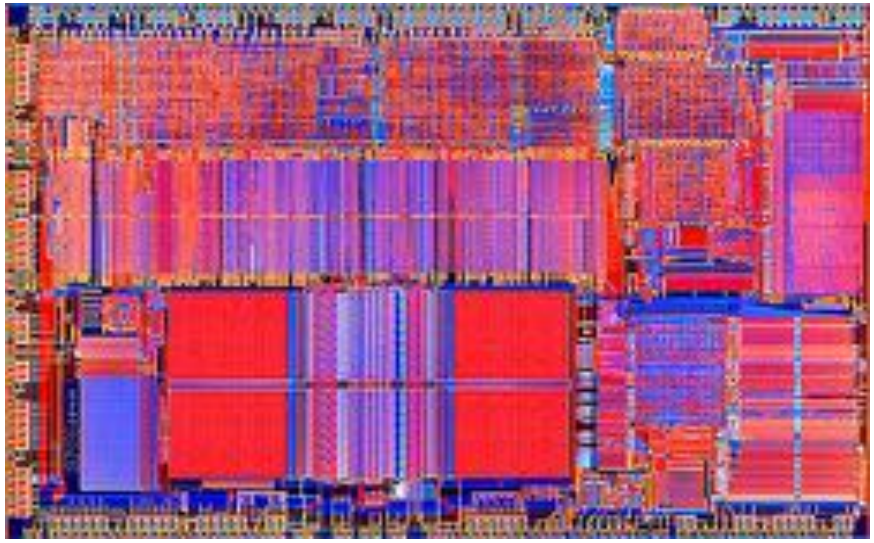
Intel 8080



Intel 8085



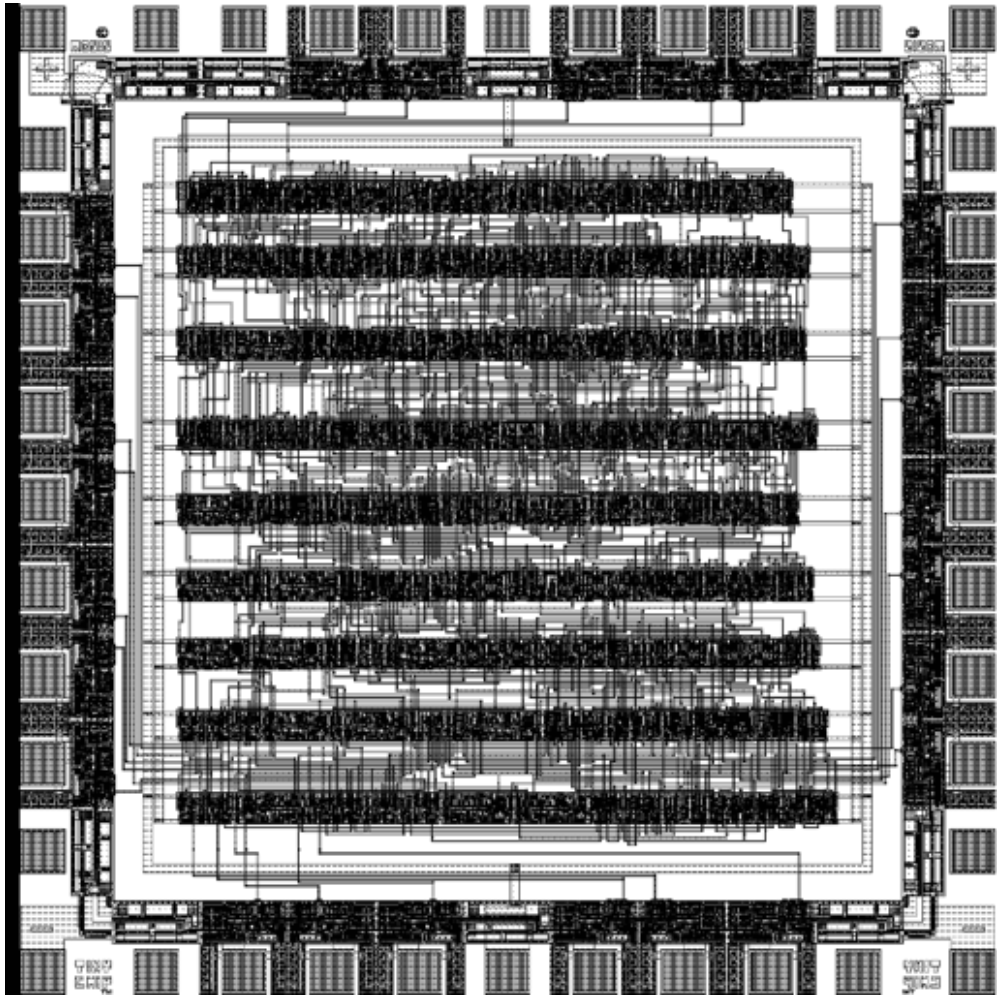
Intel 8286



Intel 8486

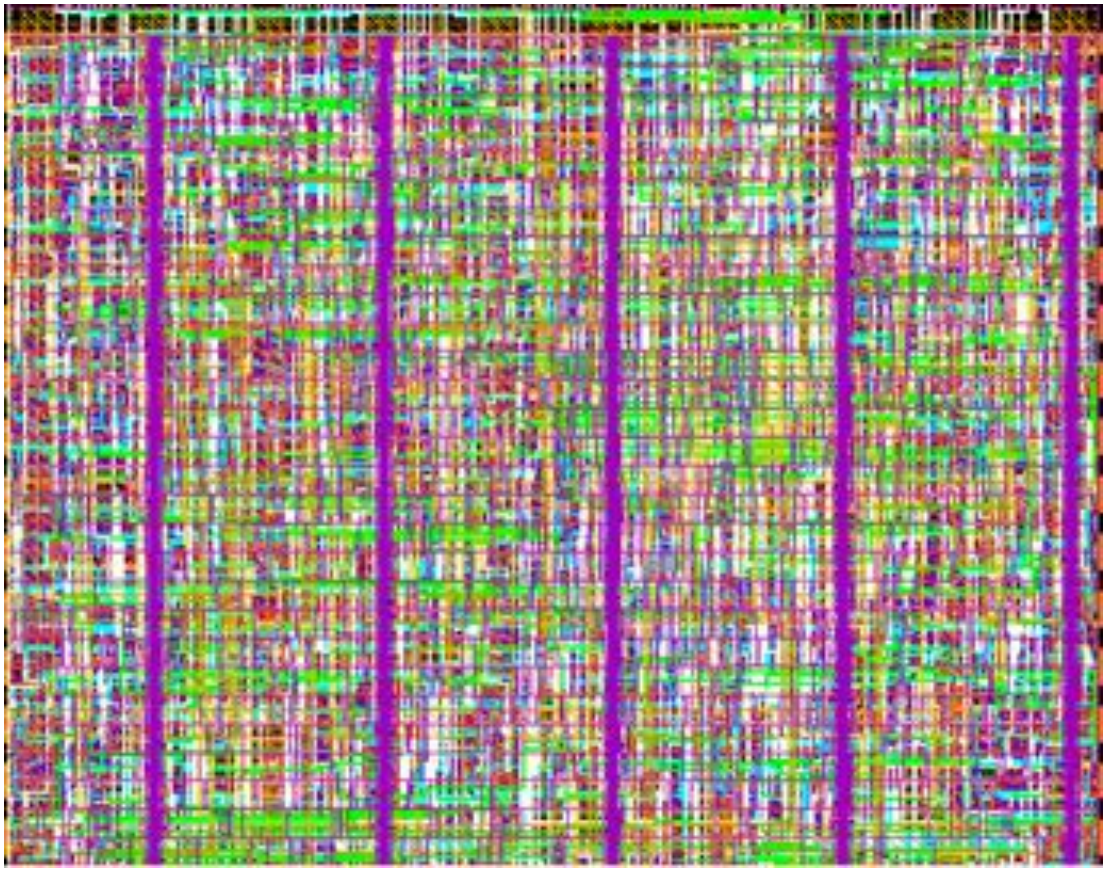
Courtesy Intel

Standard Cell — Example



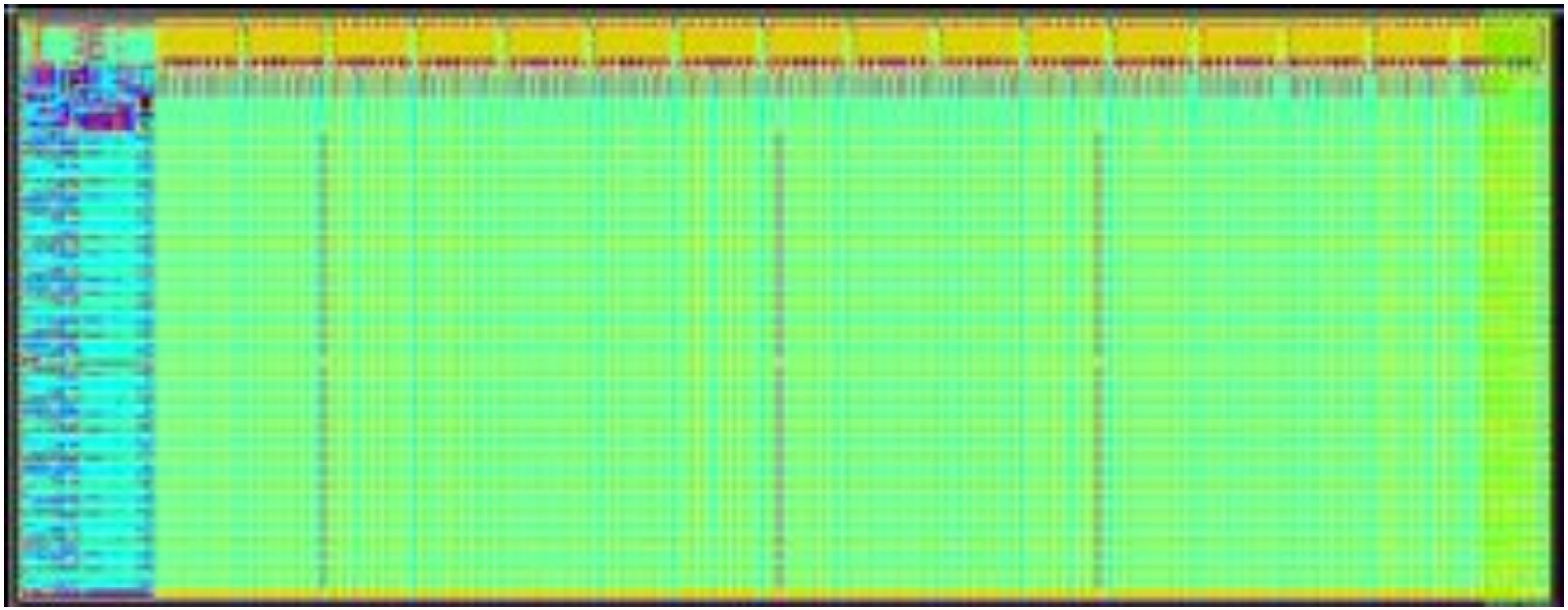
[Brodersen92]

Standard Cell – The New Generation



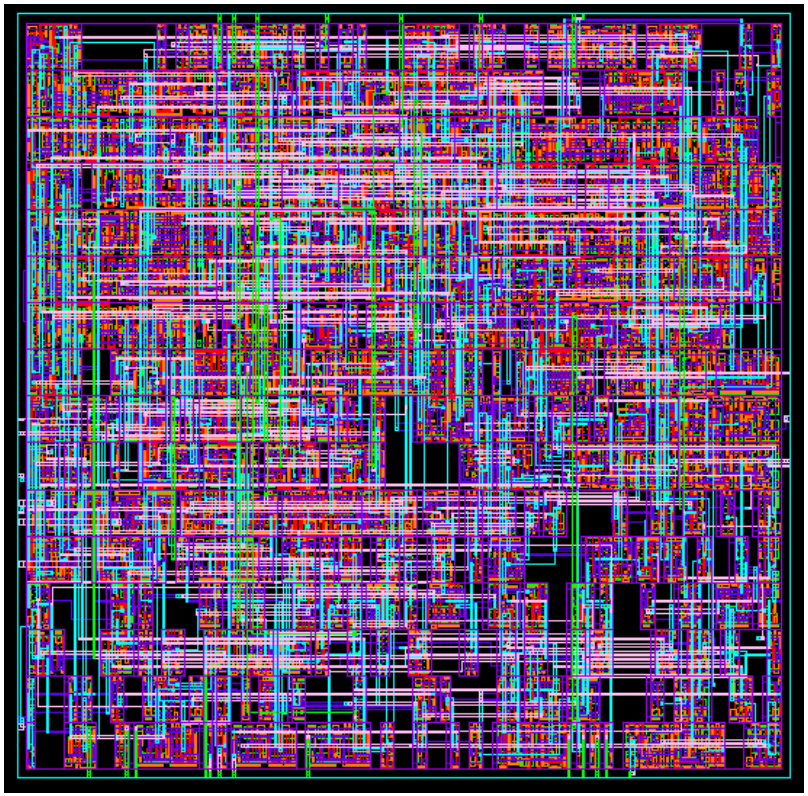
Cell-structure hidden under interconnect layers

MacroModules

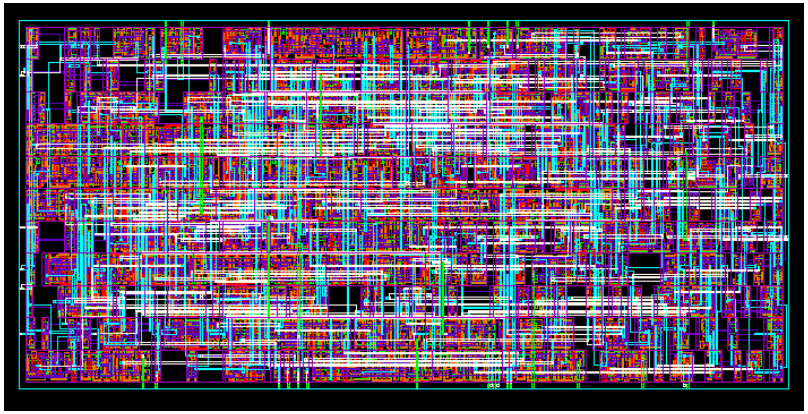


256×32 (or 8192 bit) SRAM
Generated by hard-macro module generator

“Soft” MacroModules

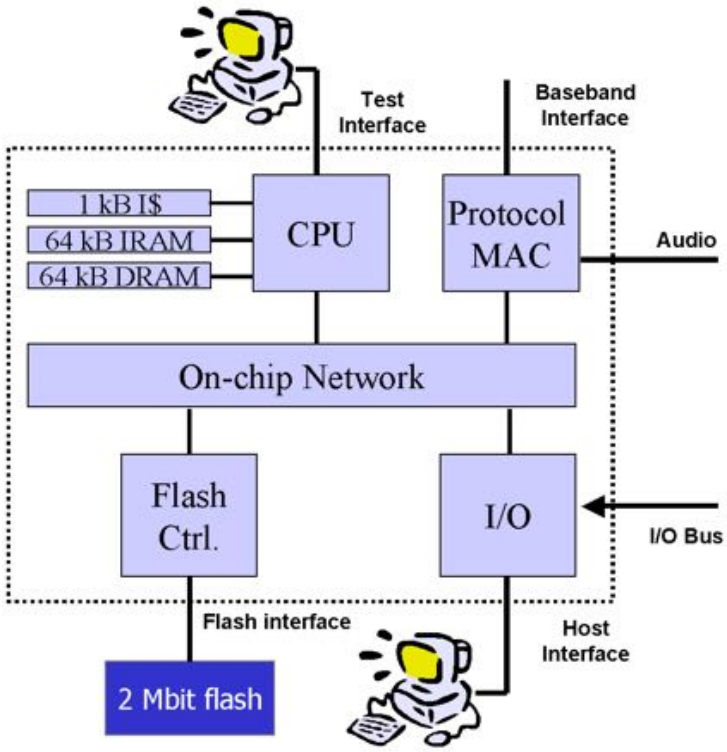


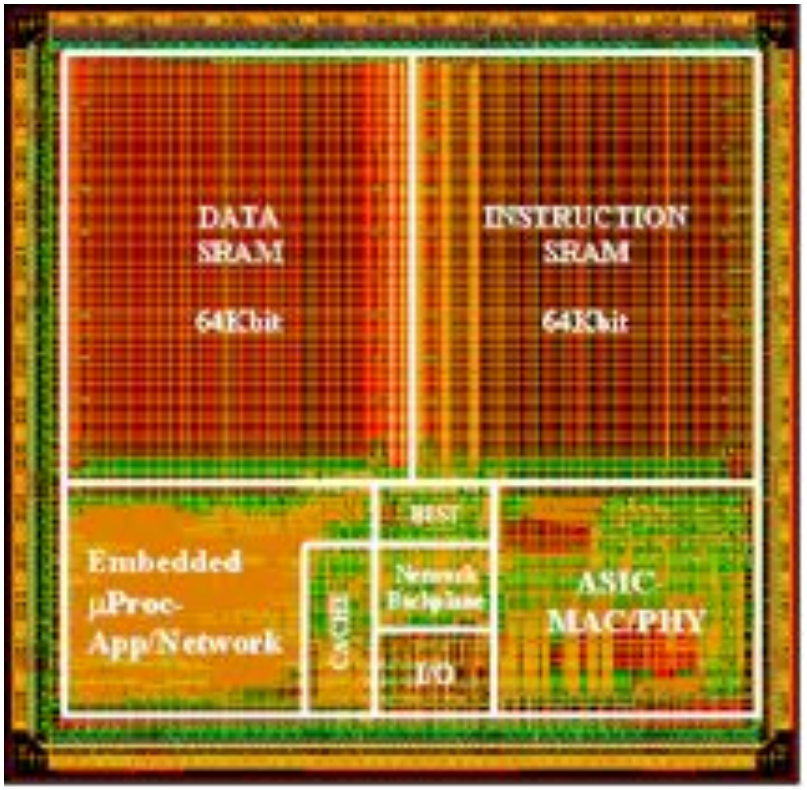
```
string mat = “booth”;
directive (multtype = mat);
output signed [16] Z = A * B;
```



Synopsys DesignCompiler

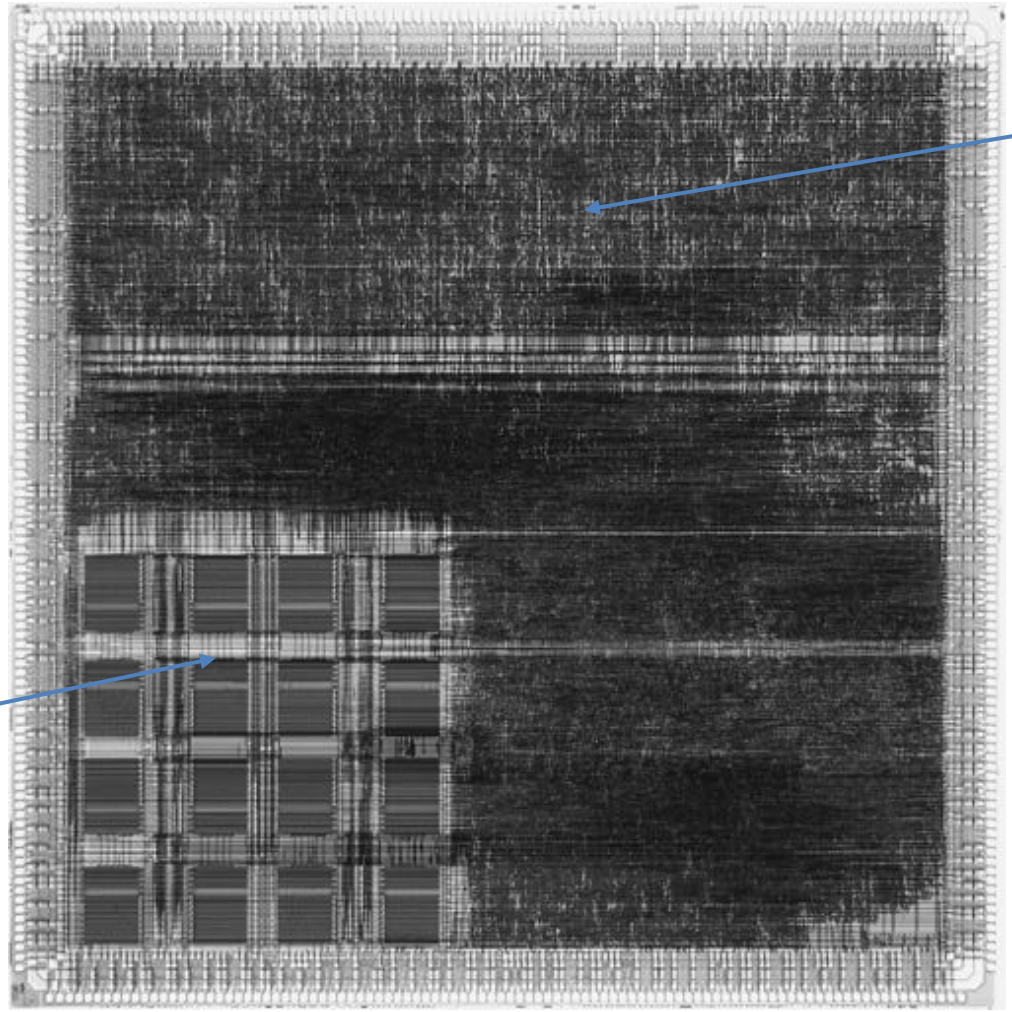
“Intellectual Property”





A Protocol Processor for Wireless

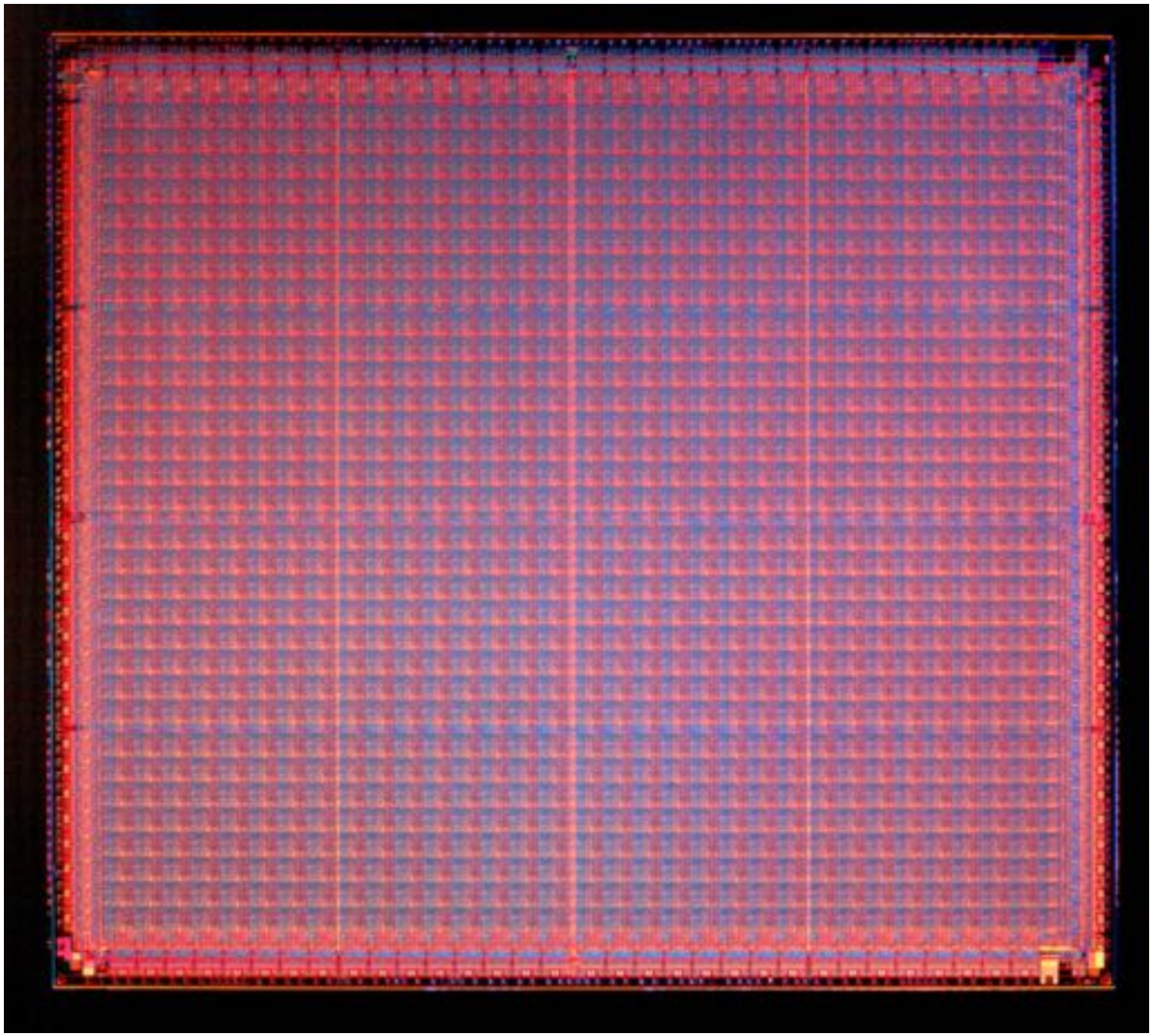
Sea-of-gates



LSI Logic LEA300K
(0.6 μm CMOS)

Courtesy LSI Logic

RAM-based FPGA



Xilinx XC4000ex

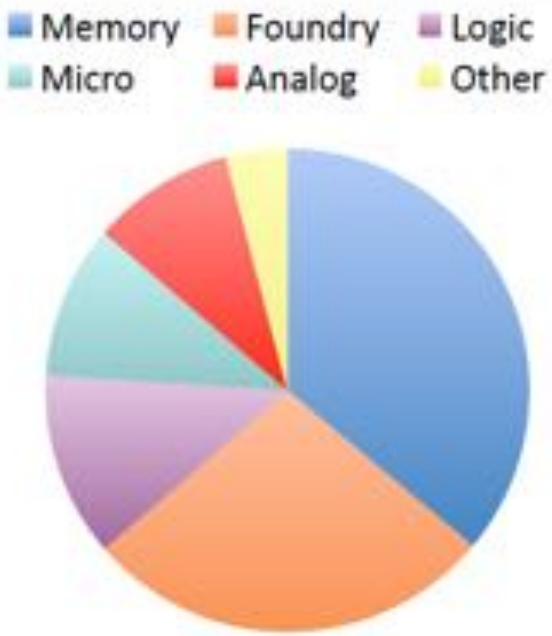
Courtesy Xilinx

Xilinx Virtex UltraScale

Value	Deliverables
Programmable System Integration	• Up to 5.5M System Logic Cells at 20nm using 2nd generation 3D IC • Integrated 100G Ethernet MAC and 150G Interlaken cores
Increased System Performance	• Up to two speed-grade improvement with high utilization • 30G transceivers for chip-to-chip, chip-to-optics, 28G backplanes • 16G backplane capable transceivers at half the power • 2,400 Mb/s DDR4 for robust operation over varying PVT
BOM Cost Reduction	• Up to 50% lower cost – half the cost per port for Nx100G systems • VCXO and fractional PLL integration reduces clocking component cost • 2,400 Mb/s DDR4 in a mid-speed grade
Total Power Reduction	• Up to 40% lower power vs. previous generation • Fine granular clock gating with ASIC-like clocking • Enhanced logic cell packing reduces dynamic power
Accelerated Design Productivity	• Footprint compatibility with Kintex UltraScale devices for scalability • Seamless footprint migration from 20nm planar to 16nm FinFET • Co-optimized with Vivado Design Suite for rapid design closure

IC Production – Installed capacity

Worldwide Capacity by Product Type as of Dec-2012
(Installed Monthly Capacity in 200mm-Equiv. Wafers x1000)



Product Type	Installed Capacity (K w/m)	% of Worldwide Total
Memory	5,237.4	36.1%
Foundry	3,990.7	27.5%
Logic	1,791.3	12.4%
Micro	1,493.8	10.3%
Analog	1,387.4	9.6%
Other	596.5	4.1%
TOTAL	14,497.0	100%

Source: IC Insights

IC Production
Breakdown by Region

Regional Capacity by Product Type as of Dec-2012
(Installed Monthly Capacity in 200mm-Equiv. Wafers x1000)

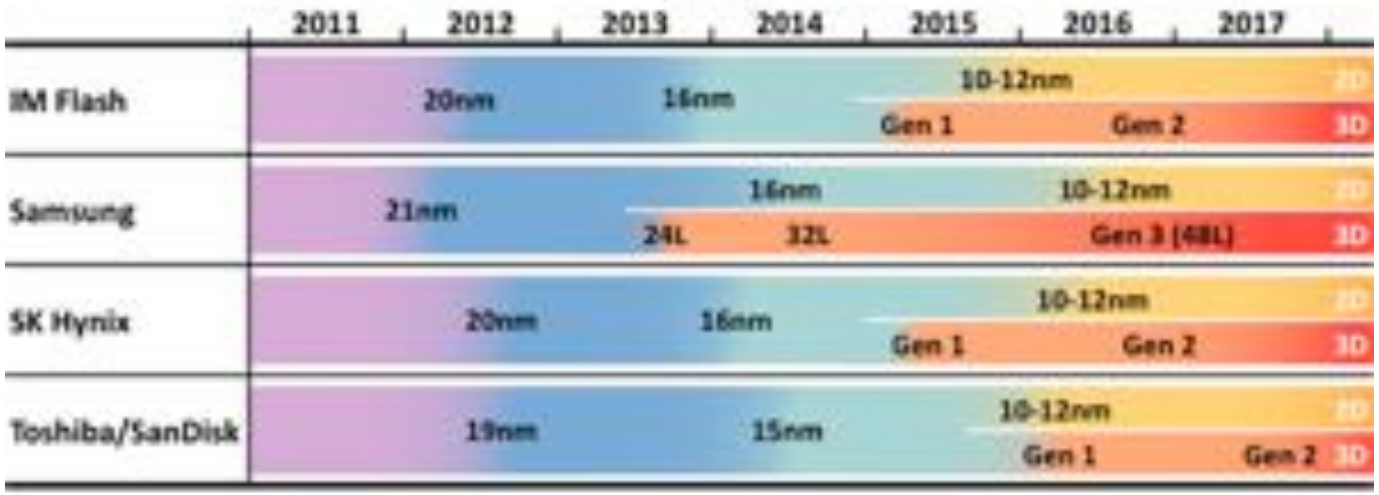
Product	Americas	Europe	Japan	Korea	Taiwan	China	ROW	Total
Analog	323.5	328.3	391.9	31.5	19.2	153.5	139.4	1,387.4
Memory	382.9	29.3	1,109.1	1,821.8	1,194.3	338.3	362.0	5,237.4
Logic	341.1	167.8	704.2	363.1	37.7	70.9	106.5	1,791.3
Micro	727.2	326.4	251.1	26.3	5.1	11.2	146.6	1,493.8
Foundry	296.5	135.5	124.5	254.6	1,899.0	737.3	543.3	3,990.7
Other	50.0	128.5	119.2	67.5	10.1	19.8	201.3	596.5
Total	2,121.3	1,115.7	2,700.1	2,564.7	3,165.4	1,330.8	1,499.0	14,497.0

Source: IC Insights

Korea, Japan ~ 2x Europe
Taiwan ~ 3x Europe

Memory roadmap

NAND Flash Process Roadmaps (for Volume Production)

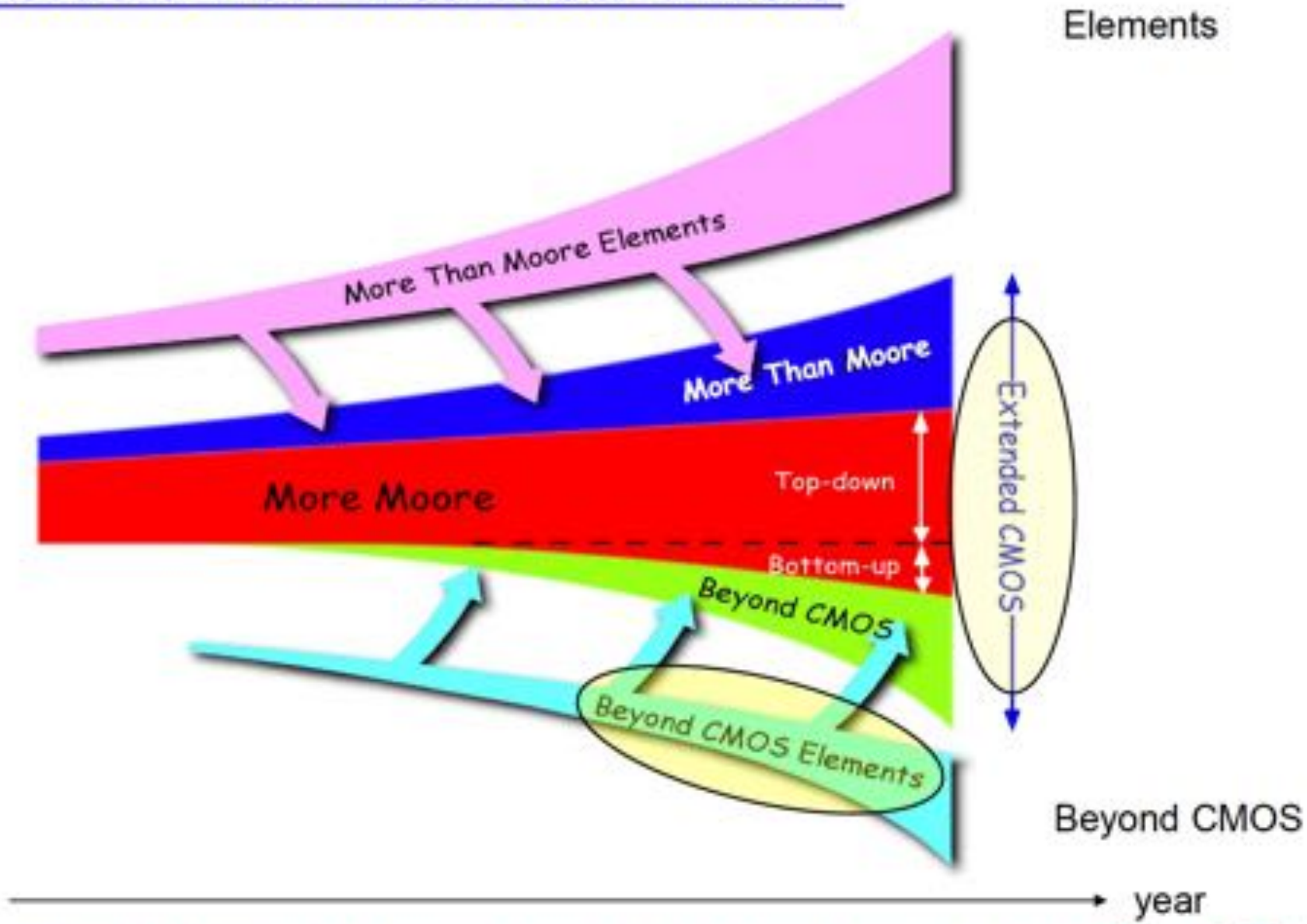


DRAM Process Roadmaps (for Volume Production)

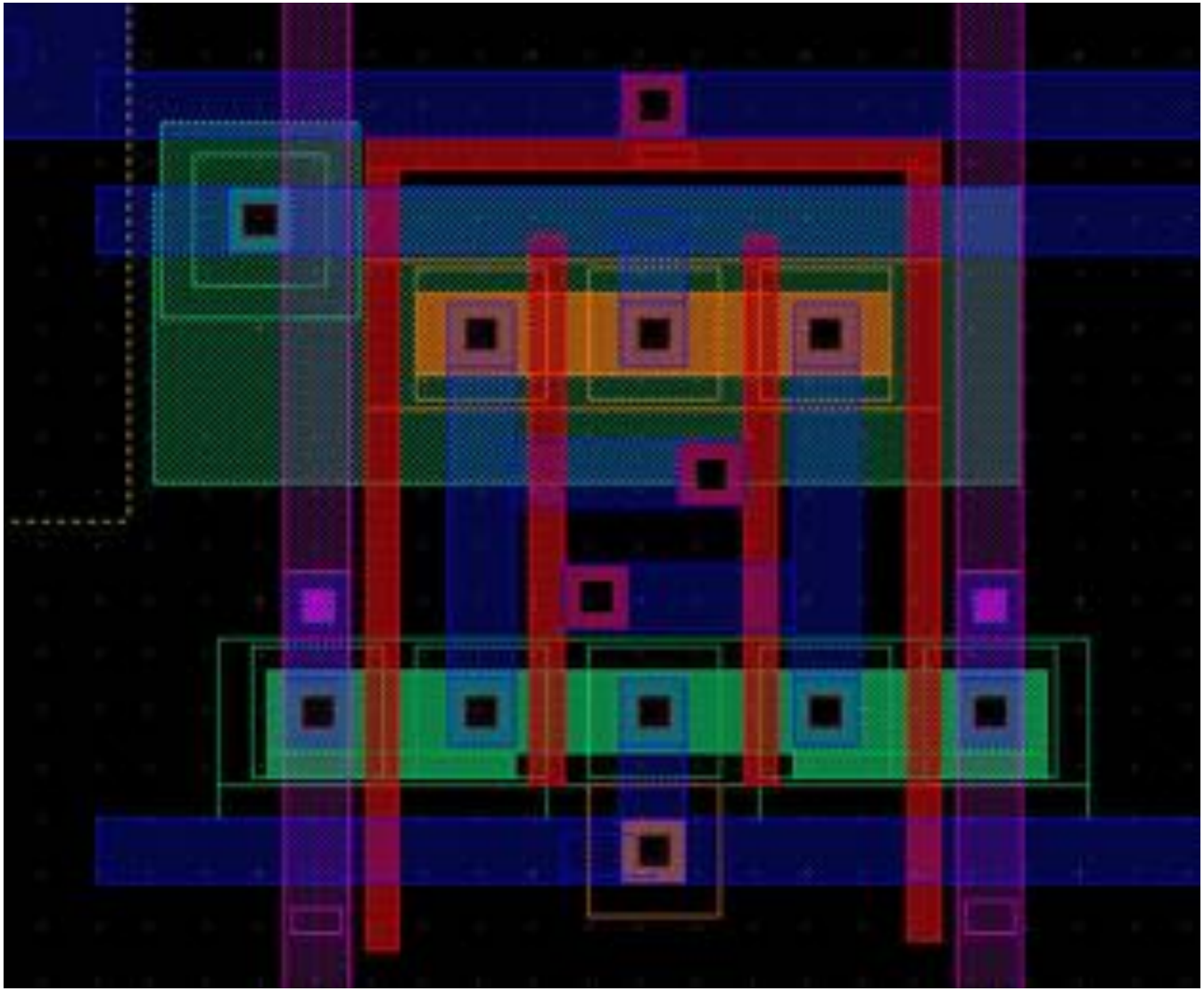
Note: What defines a process "generation" and the start of "volume" production varies from company to company, and may be influenced by marketing embellishments, so these points of transition should be used only as very general guidelines.

Sources: Companies, conference reports, IC Insights

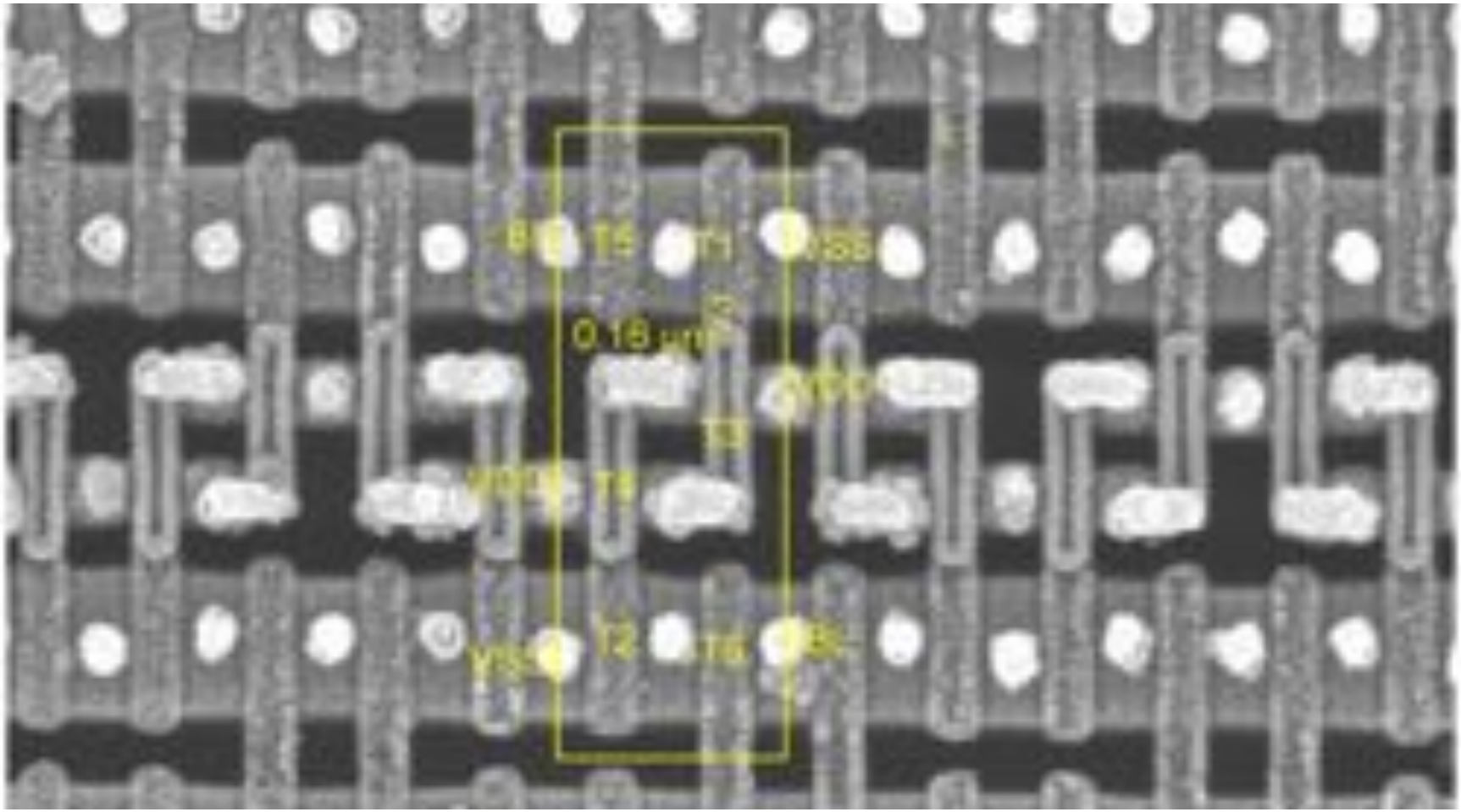
Evolution of Extended CMOS



SRAM Layout

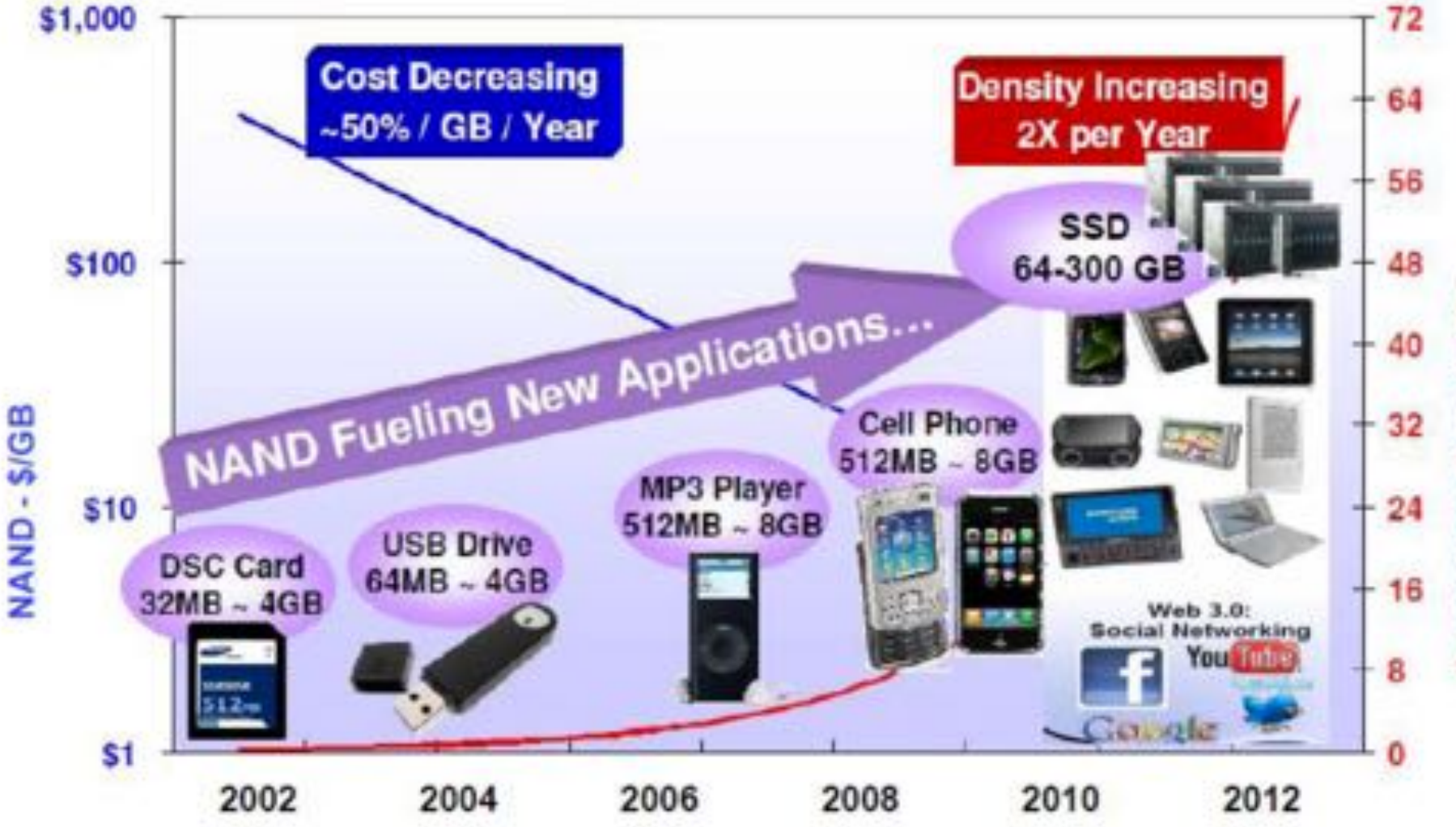


6T SRAM – 28 nm CMOS TSMC



Courtesy of Chipworks

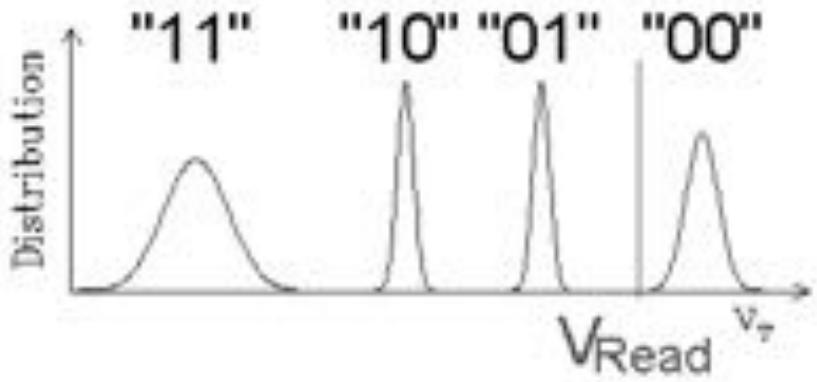
NVM Applications



Multilevel concept: 1

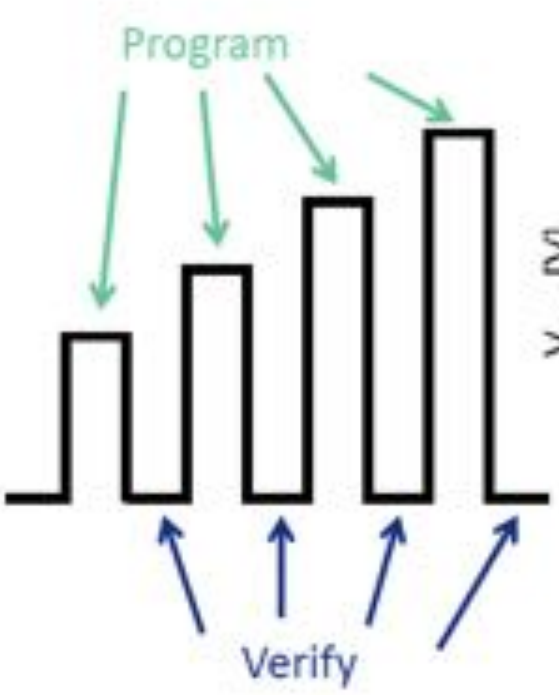
Threshold voltage distribution

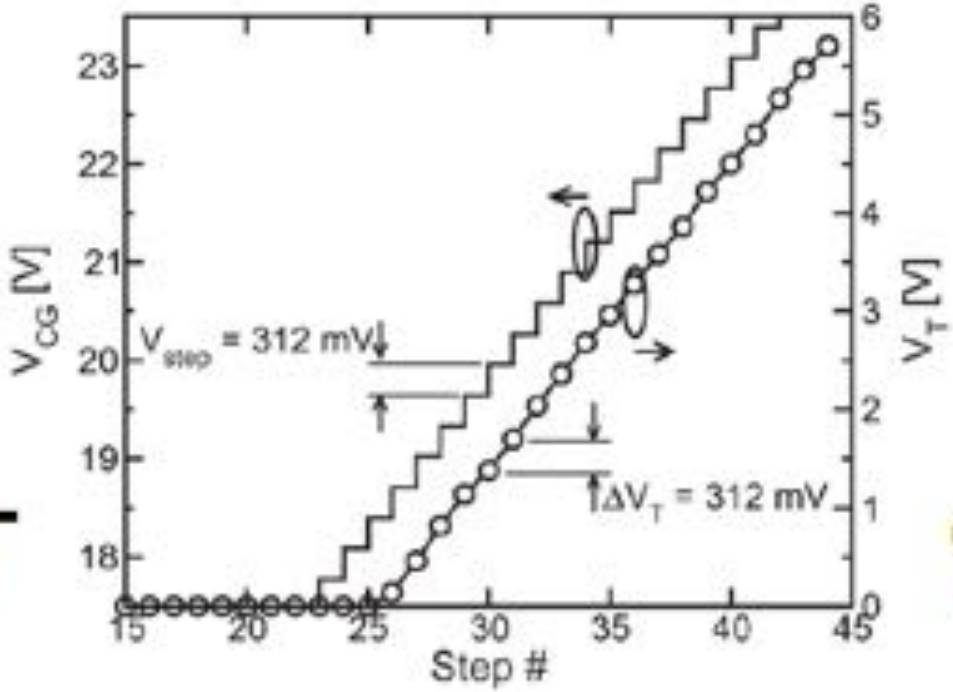
- 1 bit/cell => 2 levels



- 2 bit/cell => 4 levels

Multilevel concept:
Program and verify mechanism





From Monzio Compagnoni et al., TED (2008)

$$\Delta V_T = V_{step}$$

NAND: From gate wrap to 2D planar

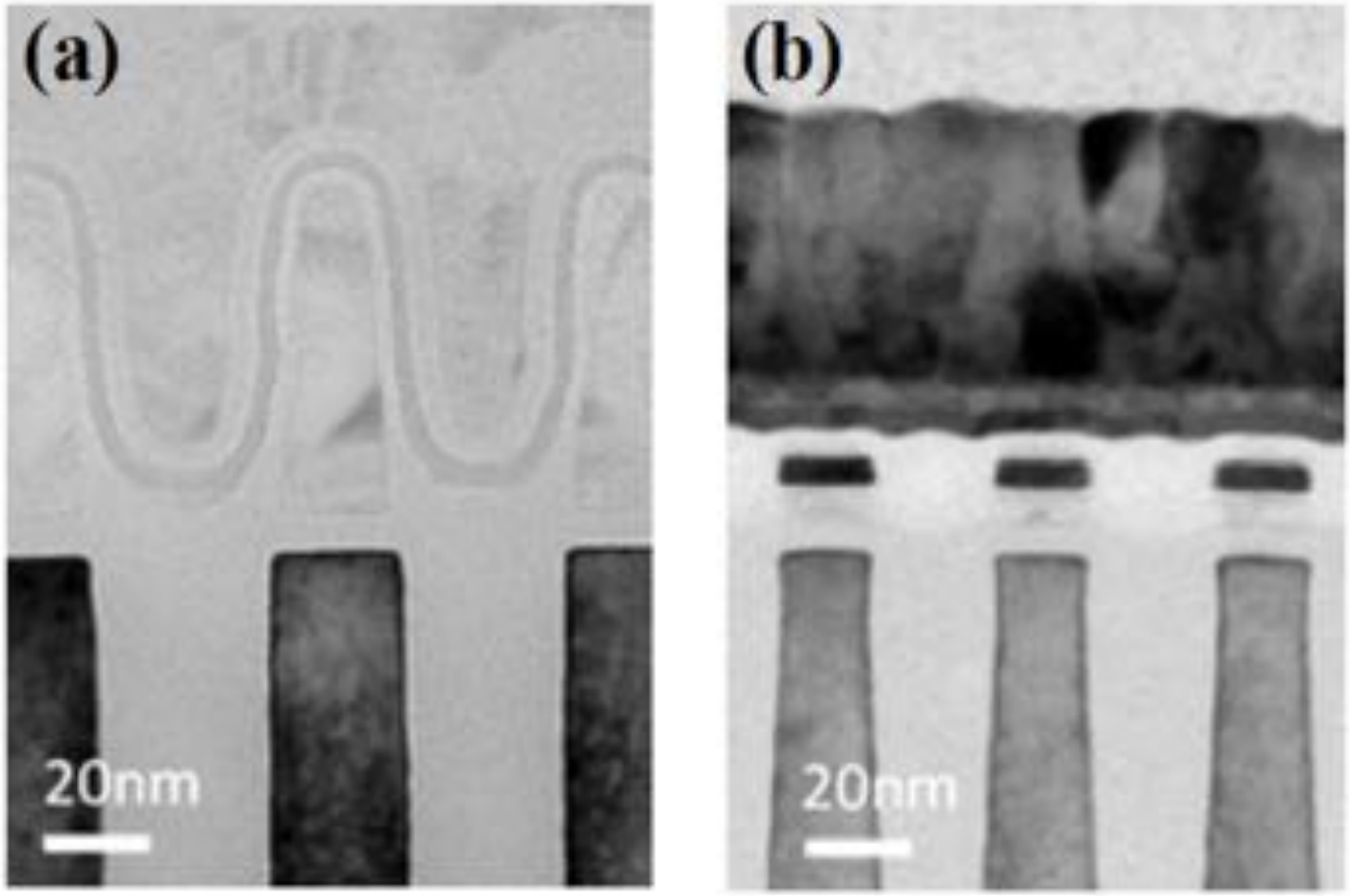
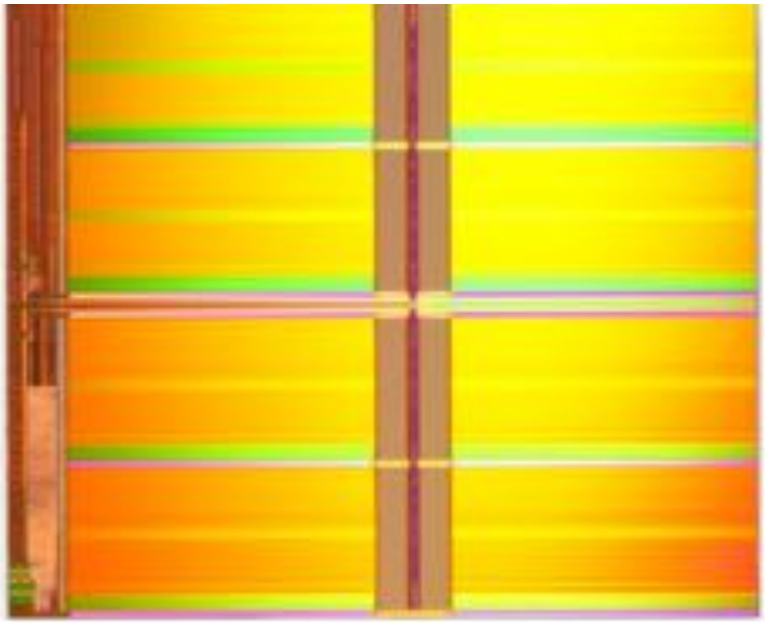
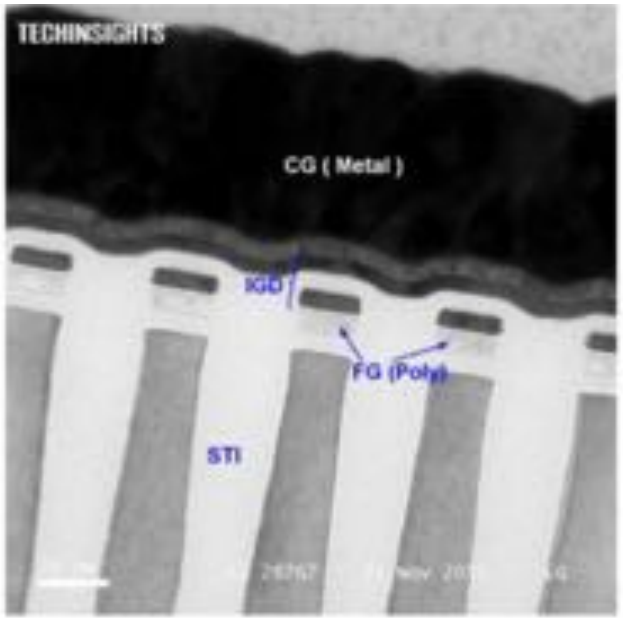


Fig. 1: Cross-sections of a conventional wrap FG cell (a) and an Intel-Micron 20nm planar FG cell (b).

A. Goda, K. Parat, IEDM 2012

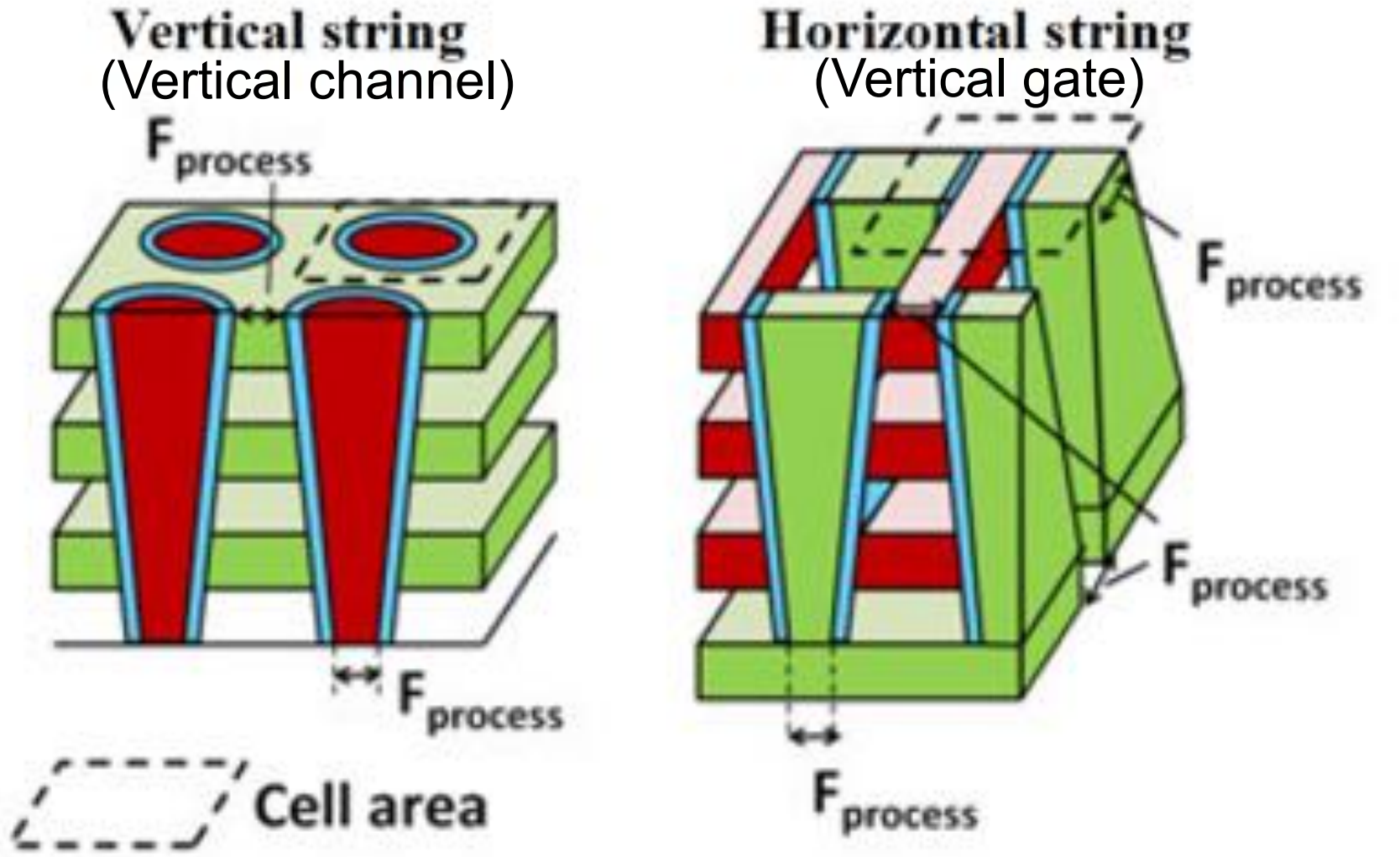
2012





- 8 GB IMFT NAND Flash
- 20 nm technology node
- More than 32 billion MOS devices in 118 mm^2

Now: 3D NAND Architectures



Power Delivery Network of a Smartphone

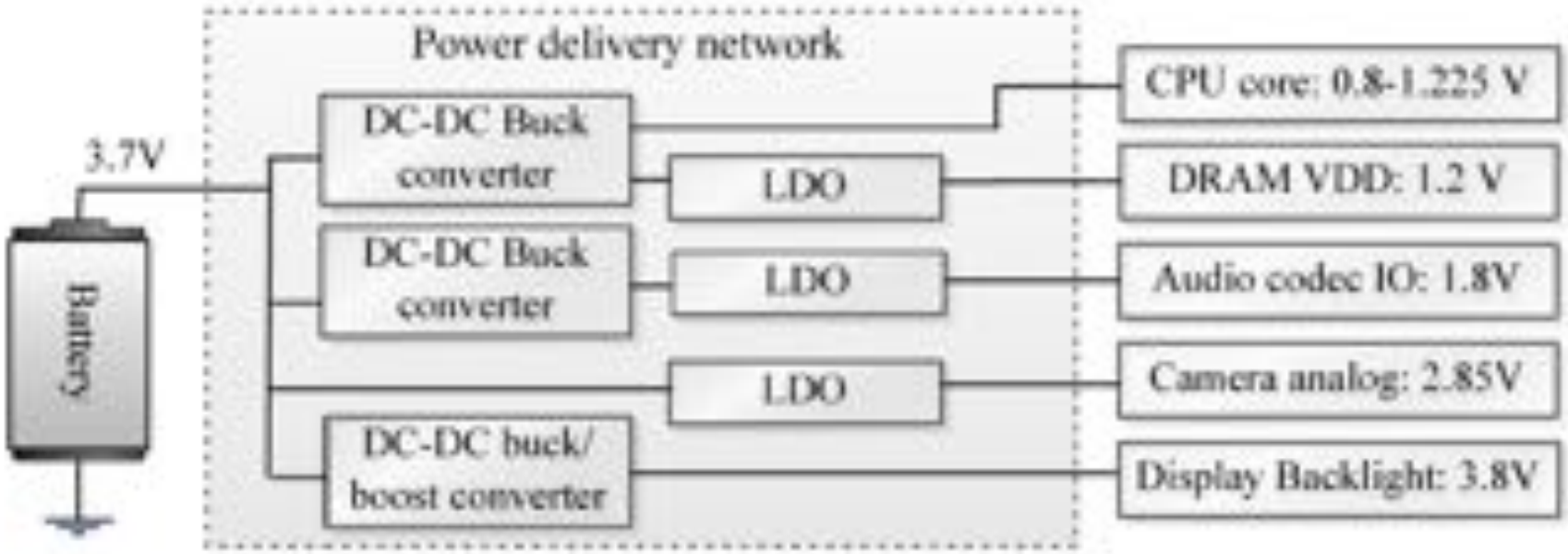


Fig. 1. Conceptual diagram of the PDN in a smartphone platform.

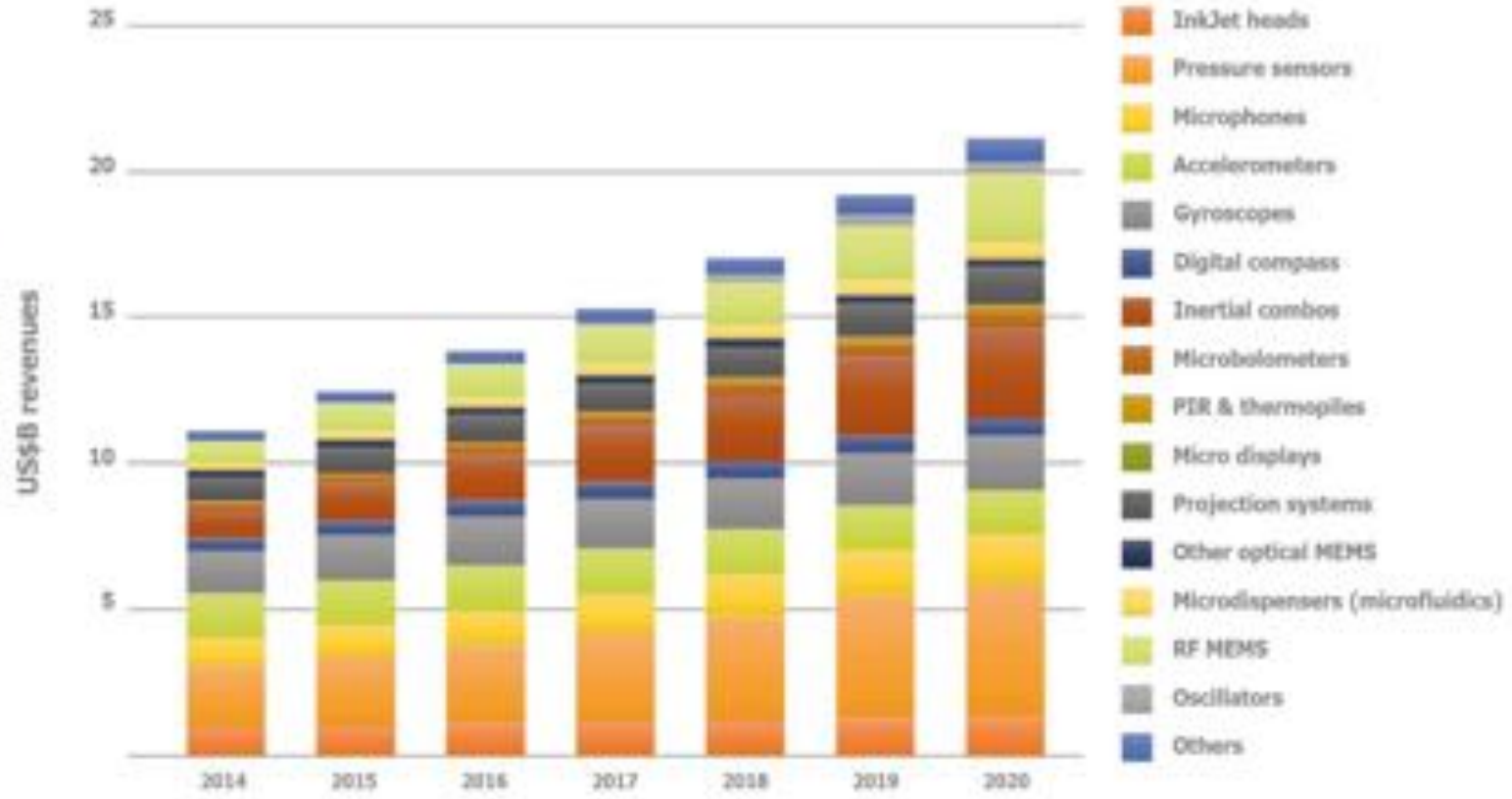
Lee et al., IEEE-TCAD Vol.33, pp, 136, 2015.

MEMS Global Market

MEMS MARKET FORECAST: 2014 – 2020 VALUE (IN B$)

(Source: Status of the MEMS Industry, Yole Développement, May 2015)

In 2014, the MEMS sector represented an $11.1B business for Si-based devices…
(Source: Yole Développement)



MEMS Gyroscopes

Traditionally used in navigation when the geomagnetic field is absent (i.e. in space) or disturbed (i.e. on a plane, in a tunnel).

NOW used in:

- Stabilization devices
- Robotics
- Tunnel Mining
- Weapons

When the GPS does not work (indoor, in space, in bad weather)

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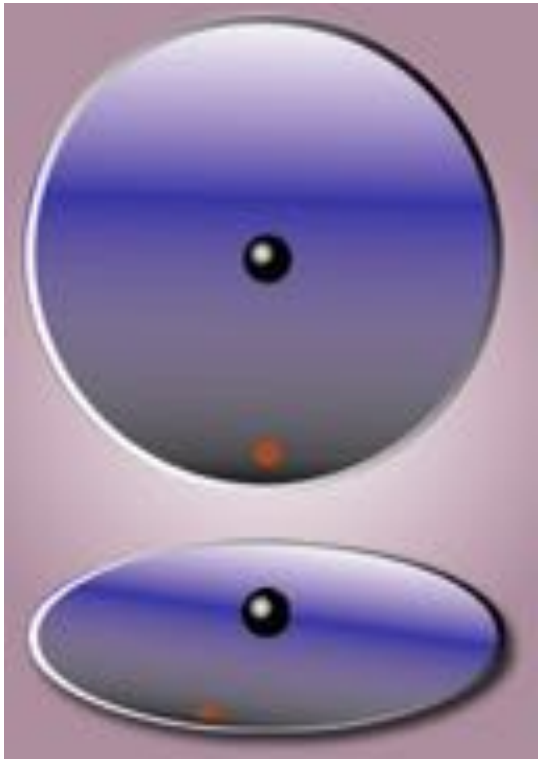
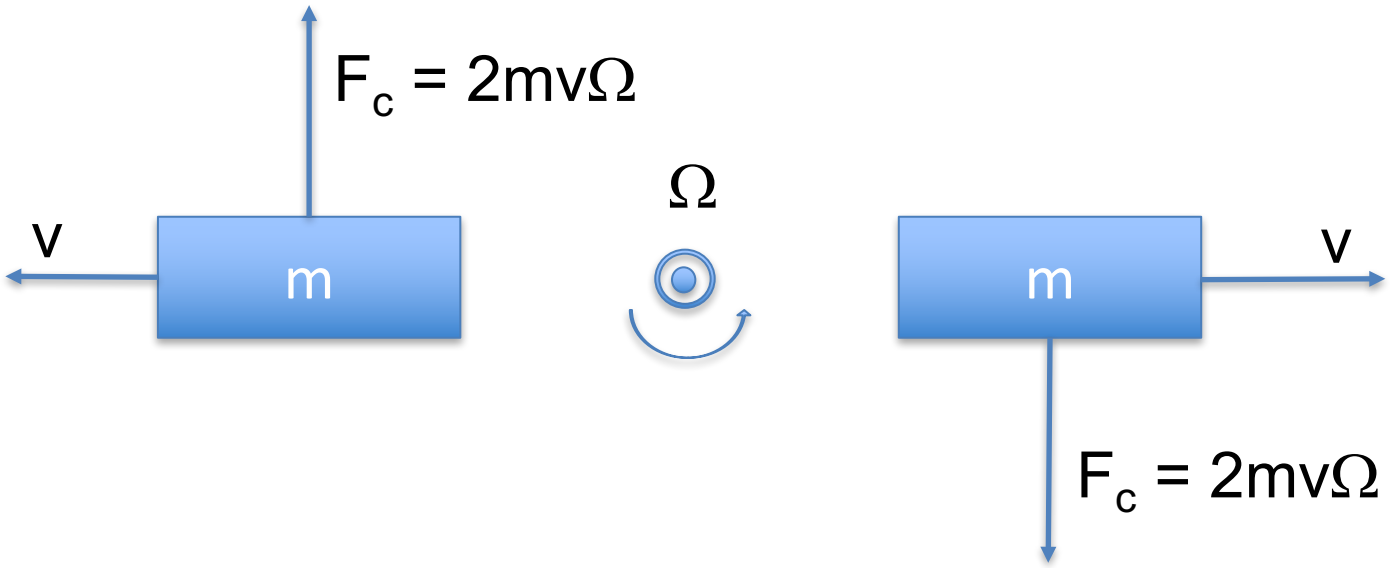
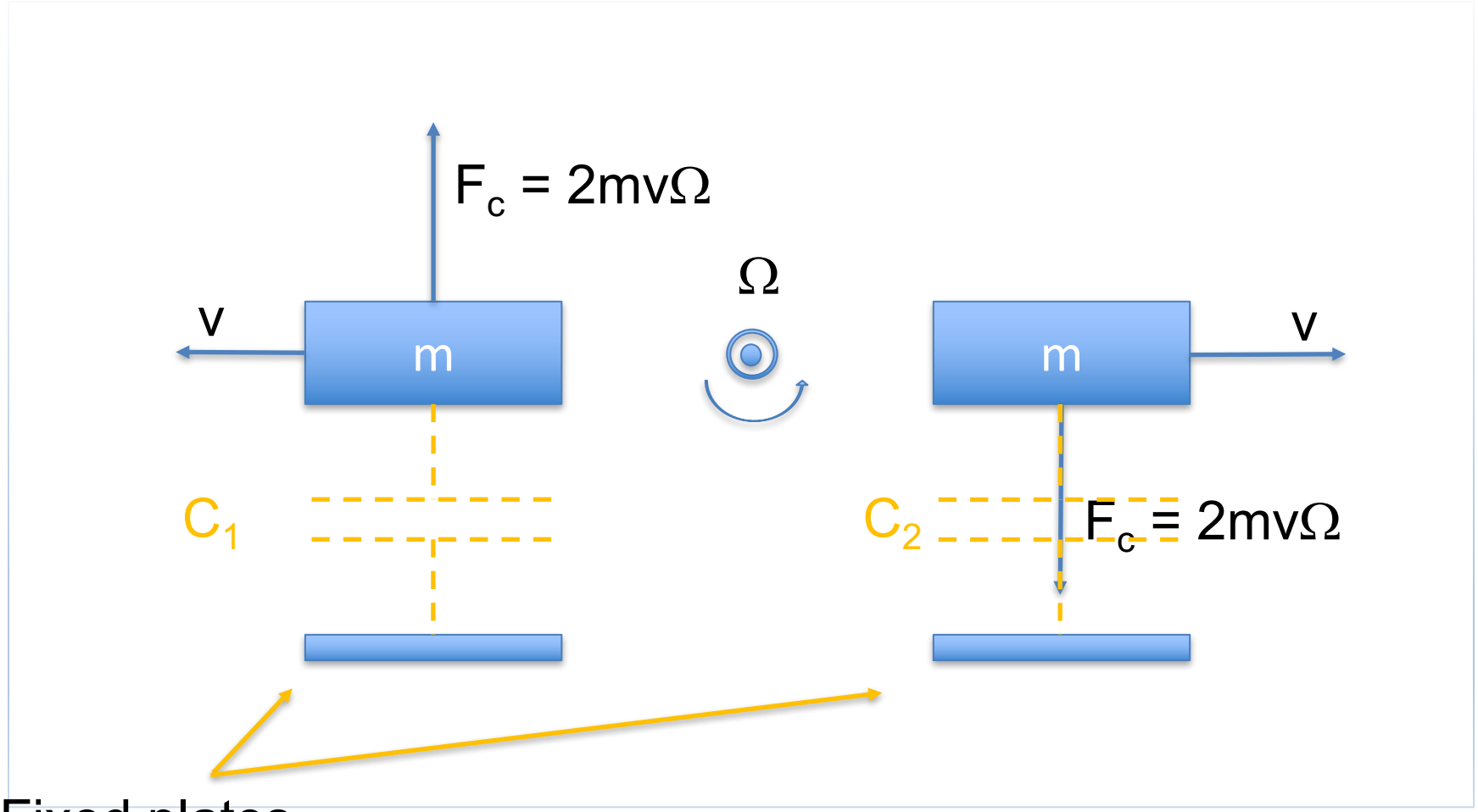


Basic 1-axis accelerometer



Basic 1-axis accelerometer



One axis accelerometer