

# Optimization and benchmarking of graphene-based heterostructure FETs

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**Abstract**— We compare the performance prospects of three recently proposed and demonstrated transistors based on vertical and lateral graphene-based heterostructures, with the requirements of the International Technology Roadmap for Semiconductors. All devices provide large  $I_{ON}/I_{OFF}$  ratios, but only the lateral heterostructure field-effect transistors exhibit promising dynamic figures of merit, i.e. delay time and power-delay-product. The assessment is based on numerical simulations using our in-house nanoscale device simulation tool NanoTCAD Vides.

**Keywords**—nanoelectronics, graphene transistors; device simulation; TCAD; heterostructures.

## I. INTRODUCTION

Native graphene has a zero energy gap and it is therefore not suitable as a transistor channel material for digital electronics [1]. However, recent advances based on materials engineering have demonstrated graphene-based “materials on demand”, with tailored properties [2,3]. Vertical graphene heterostructures have been proven to be suitable for FETs [4,5] and hot-electron transistors [6] exhibiting large current modulation [7].

Inspired by recent progress in the growth of seamless lateral graphene heterostructures [8-10], graphene-based lateral heterostructure (LH)-FETs have been proposed [11-13] and later demonstrated in experiments [14], exhibiting extremely promising switching behavior in terms of leakage current, propagation delay, and power-delay product.

In this work, we explore the performance potential of vertical and lateral graphene-based heterostructure transistors, which have already been demonstrated to provide large  $I_{ON}/I_{OFF}$  ratios. We use a benchmark the predictions of the International Technology Roadmap for Semiconductors (ITRS) [12], shown in Table I.

As far as devices are concerned, we focus on the lateral heterostructure FET (LH-FET), and two FETs based on vertical graphene-based heterostructures: one proposed by Britnell et al. [4], that we call VH-FET, and the “barristor” proposed in [15]. The three device structures are shown in Figs. 1a-c. Device simulation has been performed with our open source package NanoTCAD Vides, implementing the self-consistent solution of the Poisson and the Schrodinger equation within the Non-Equilibrium Green's Function formalism.

The considered figures of merit are:

- The  $I_{ON}/I_{OFF}$  ratio, i.e. the ratio of the drain current in the “ON” state (when  $V_{GS} = V_{DS} = V_{DD}$ , where  $V_{DD}$  is the supply voltage), to the drain current in the “OFF” state (when  $V_{GS} = 0$  and  $V_{DS} = V_{DD}$ ). According to the ITRS this ratio has to be larger than  $10^4$ , ensuring a good balance between static and dynamic power consumption
- The delay time  $t$ , which is defined as

$$\tau = \frac{Q_{ON} - Q_{OFF}}{I_{ON}}$$

where  $Q_{ON}$  and  $Q_{OFF}$  are the total charge in the device in the “ON” and “OFF” states, respectively. The delay time is a measure of switching speed.

- The Power-Delay Product (PDP), which is defined as  $PDP = V_{DD} I_{ON} \tau$ , and is a measure of energy efficiency, proportional to the energy required to switch a logic gate.

## II. RESULTS

### A. Vertical Heterostructure FET Performance

We consider the VH-FET shown in Fig. 1b, experimentally demonstrated in [4-5] and also analyzed in [7]. The source and the drain are two graphene sheets, and are separated by a thin dielectric barrier. Barrier height is modulated via the voltage applied to external metal gates, exploiting the fact that graphene is not an ideal metal, and screen only partially the electric field due to the gate voltage. The barrier consists of three atomic layers of boron-carbon-nitride, AB-stacked on graphene. Fig. 2 shows the pFET transfer characteristics for different valence band edge barriers BV. Performance figures shown are poor: the  $I_{ON}/I_{OFF}$  ratio is smaller than 20 and the delay time (not shown) is four orders of magnitude larger than that expected from ITRS. By increasing the barrier thickness to 5 monolayers, one can obtain an  $I_{ON}/I_{OFF}$  ratio larger than 1000, at the price of an even larger delay time.

### B. Barristor Performance

The barristor structure is shown in Fig. 1c. It is basically a Schottky diode where graphene is the metal electron. The Schottky barrier height is modulated via the voltage applied on gate metal gate on top of the graphene electrode, separated by a dielectric layer. Also in this case, the modulation is effective because graphene is not an ideal metal, i.e. it has a limited density of states. Silicon has a donor doping  $N_D$  and the gate dielectric has effective oxide thickness EOT. Fig. 3 shows that

prospective performance is much worse than that required by the ITRS for CMOS technology. The  $I_{ON}/I_{OFF}$  can be larger than  $10^4$  for very thin EOT of the dielectric layer, but the delay time  $\tau$  and the Power Delay Product miss the target by few orders of magnitude.

### C. LH-FET Optimization and performance

Finally, we consider the double-gate p-channel LH-FET illustrated in Fig. 1a, BC2N is lattice-matched to graphene and has a bandgap of 1.6 eV, offering a barrier to holes from graphene of 0.64 eV. As can be seen in Fig. 4a, the transfer characteristics are almost independent of  $t_B$ , and all performance parameters are optimized when  $t_B = L$  (Figs. 4b). As can be seen, in this case,  $I_{ON}/I_{OFF}$  is very large ( $>10^4$ ) and complying with ITRS requirements, and outperforming VH-FET and the Barristor.

Finally, we compare in Fig. 5 the delay time and the PDP of the LH-FET with the requirements of ITRS 2012 for high performance logic CMOS [12]. As can be seen, LH-FETs exhibit lower intrinsic delay time and lower  $\tau$  than CMOS for the same gate length (considering 10 nm for 2020, and 7 nm for 2024). The VH-FET and barristor cannot be included in the comparison since they exhibit larger delay times by at least three orders of magnitude.

## III. DISCUSSION

There is an intrinsic reason that explains why the vertical devices considered here have poor dynamic performance. Indeed, the operating mechanisms of both the barristor and the VH-FET are based on the fact that graphene is not an ideal metal, so that the barrier can be modulated by the gate voltage, even if there is a graphene sheet between the gate and the barrier. On the other hand, graphene partially screens the electric field, and therefore barrier modulation by the gate voltage is not very efficient. Since the gate layer is very close to and on top of the graphene sheet, there is a intrinsically large gate capacitance, which leads to a large delay time, and therefore a large Power delay product. In the lateral devices, instead, the gate is on top of a semiconducting region (the central part of the channel), and therefore the gate capacitance in the subthreshold region is much smaller.

We need to highlight the fact that our simulations consider ideal (defectless) devices, in which energy dissipation in transport is present occurs only in the contacts. More realistic assumptions on scattering and dissipation typically reduce the  $I_{ON}$  by a factor two. Even taking this aspect into account, graphene-based lateral heterostructure FETs stand out as the most promising graphene-based transistors for digital electronics.

## ACKNOWLEDGMENT

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TABLE I. DATA EXTRACTED FROM THE REQUIREMENTS OF CMOS TECHNOLOGY ACCORDING TO THE 2012 EDITION OF THE ITRS ROADMAP. HP MEANS HIGH PERFORMANCE TECHNOLOGY, LP MEANS LOW OPERATING POWER TECHNOLOGY. THE YEAR CORRESPONDS TO THE FIRST YEAR OF TECHNOLOGY SHIPPING

	HP2014	LP2014	HP2018	LP2018	HP2026	LP2026
Channel length (nm)	18	19	12.8	13.1	5.9	5.8
$V_{DD}$ (V)	0.82	0.65	0.73	0.57	0.57	0.43
$I_{off}$ (nA/ $\mu$ A)	100	5	100	5	100	5
$I_{on}$ ( $\mu$ A/ $\mu$ A)	1573	765	1805	794	2308	666
PDP (fJ/ $\mu$ m)	0.47	0.29	0.31	0.18	0.14	0.07
$\tau$ (ps)	0.361	0.58	0.24	0.4	0.1	0.26
$I_{on}/I_{off}$	15730	153000	18050	158800	23080	133200

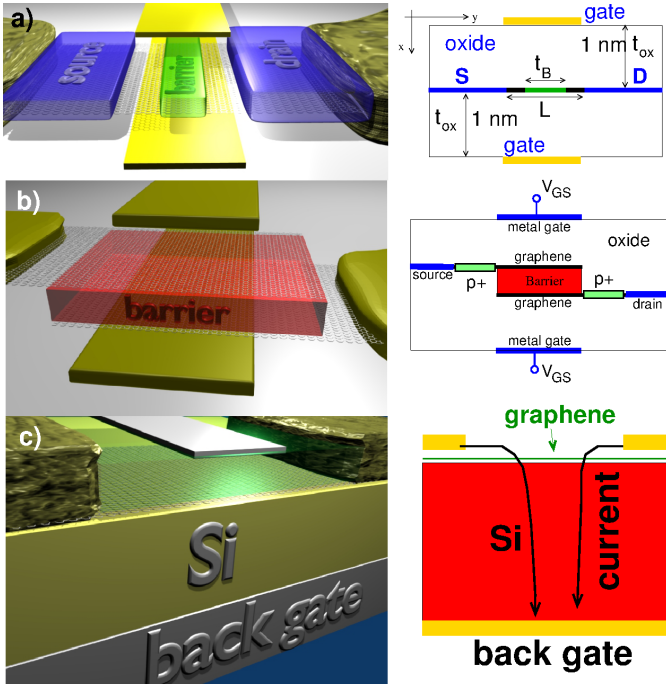


Fig. 1. Device structure of a) LH-FET; b) VH-FET; c) Barristor.

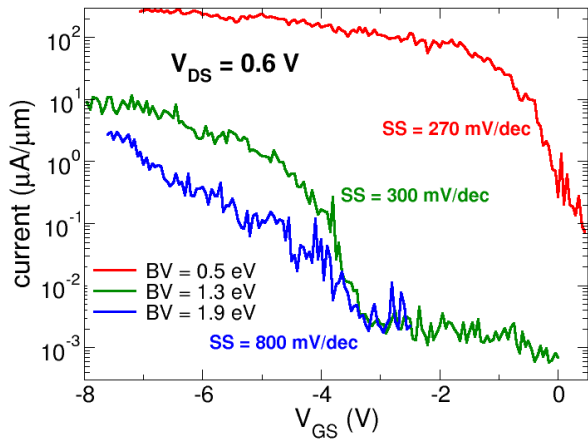


Fig. 2. Transfer characteristics of the VH-FET of Fig. 1b, for different values of the barrier BV at the valence band edge. The device has EOT = 0.62 nm (4nm HfO<sub>2</sub>), barrier thickness of three atomic layers

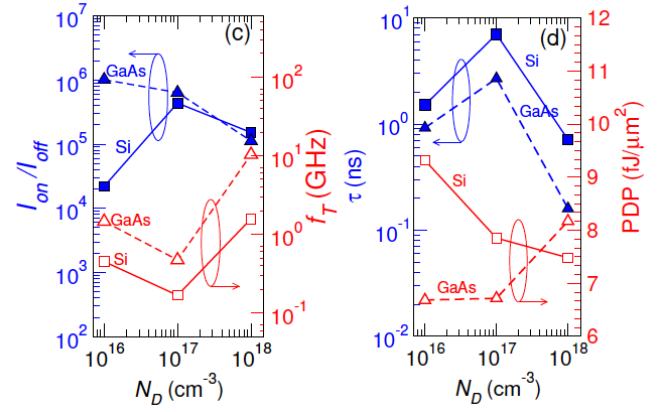


Fig. 3. left) Ion/Ioff and transition frequency  $f_T$  as a function of doping; right) delay time and PDP as a function of doping for the barristor (for EOT = 0.61 nm and different semiconductors).

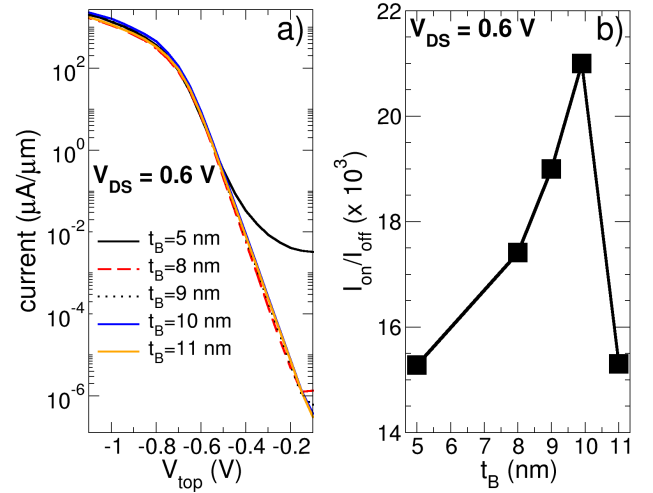


Fig. 4. a) Transfer characteristics of the LH-FET for different values of  $t_B$ . b) Ion/Ioff ratio as a function of  $t_B$ . The device has the structure shown in Fig. 1a, with  $L=10$  nm,  $t_{ox}=1$  nm,  $V_{dd}=0.6$  V,  $f=0.01$ .

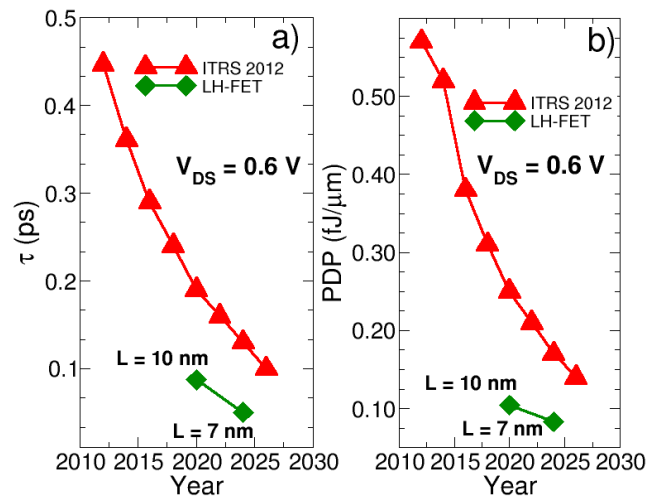


Fig. 5. a) Intrinsic delay time  $\tau$  and b) DPI as a function of year of shipment according to the ITRS 2012. On the same plot: comparison with simulation results for the LH-FETs with metal gate length of 10 nm (year 2020) and 7 nm (year 2024)